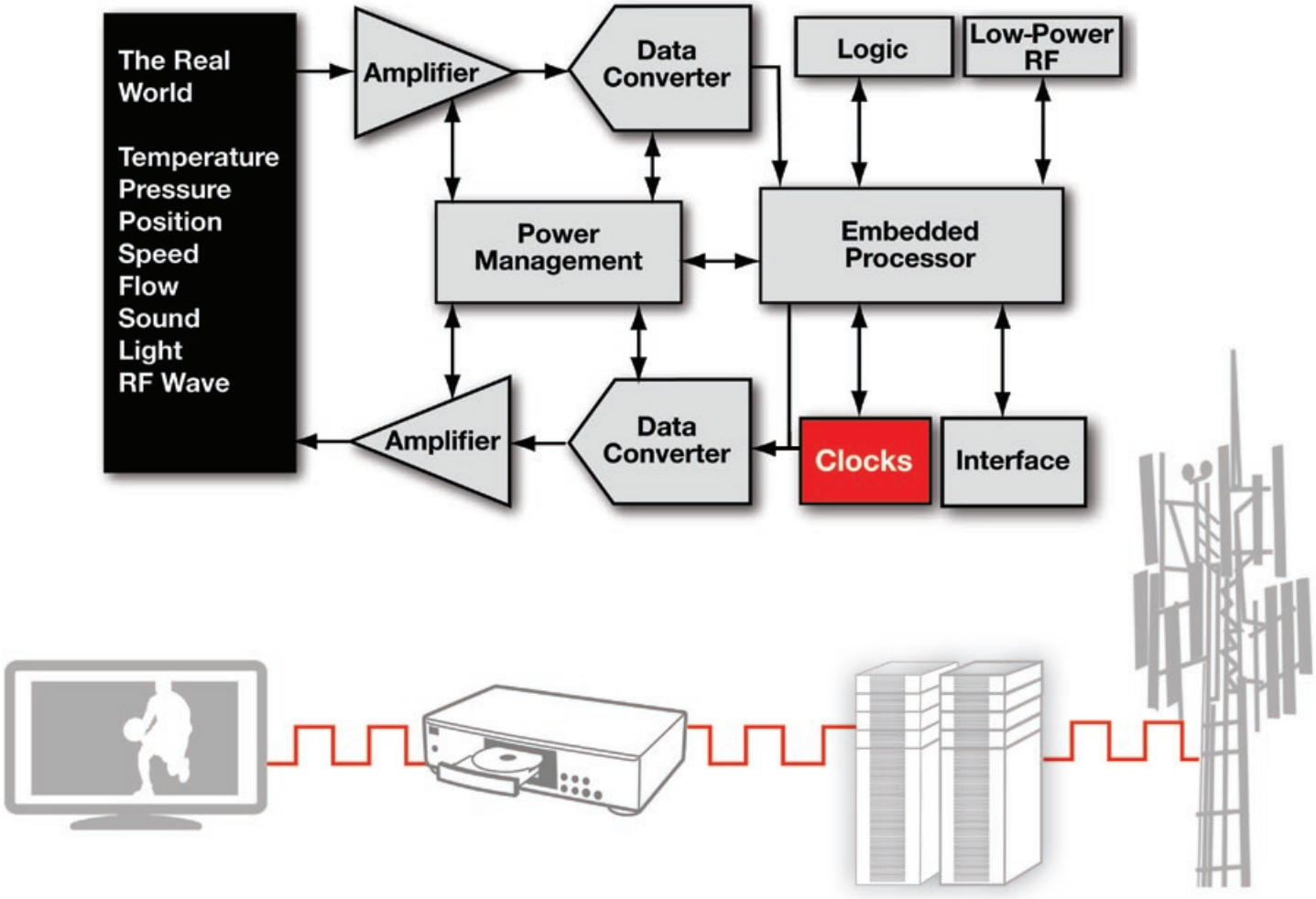
Clocks and Timing Guide

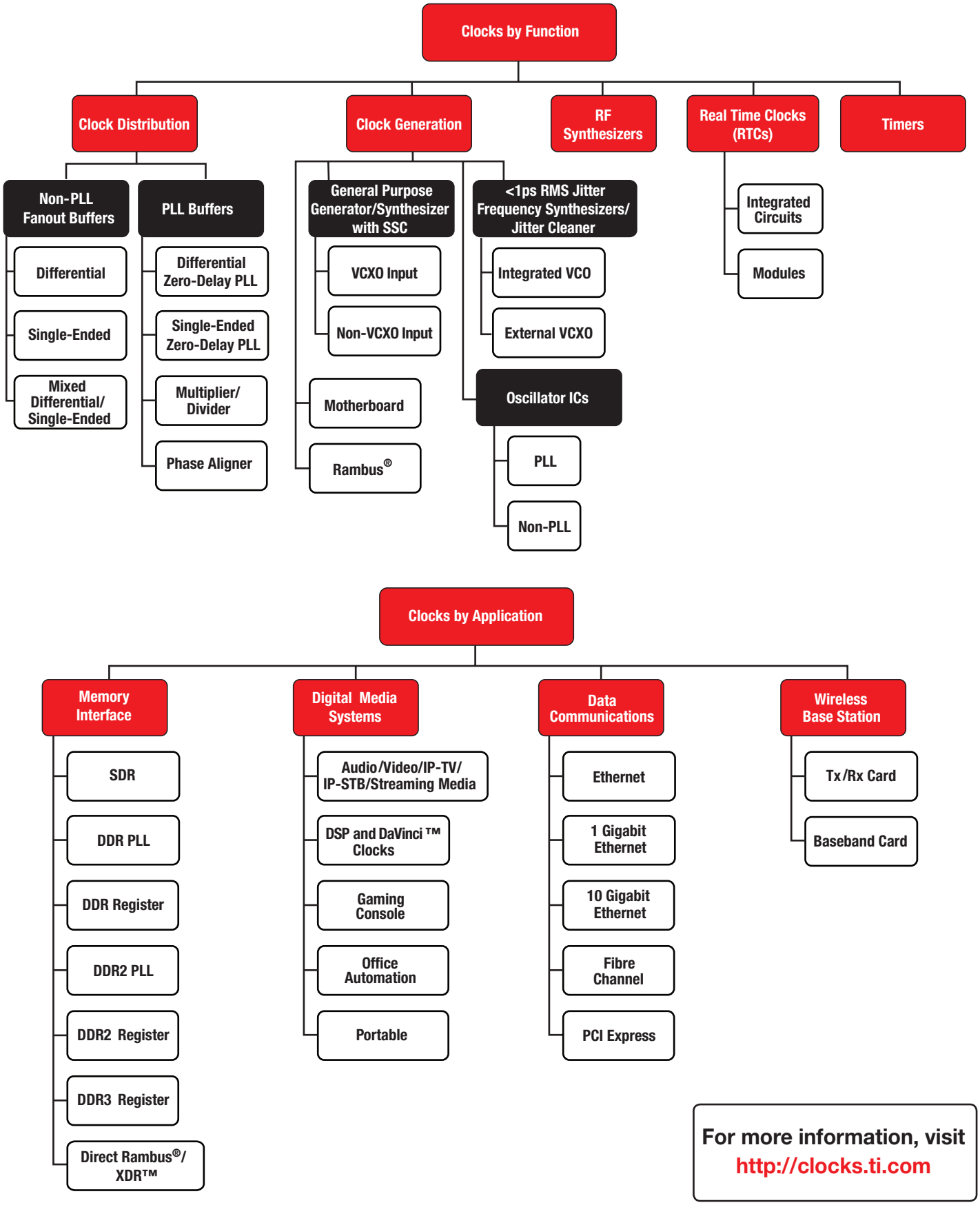
Texas Instruments



www.ti.com/clocks

2Q 2009

Clocks and Timing Selection Tree



For more information, visit
http://clocks.ti.com

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Introduction

Texas Instruments (TI) offers a wide selection of timing support devices, from non-PLL-based buffers to high-performance synthesizers and jitter cleaners. Included in the TI clock family are zero-delay PLL clock drivers and a series of PLL-based multipliers and dividers designed to help manage clock jitter and skew for a variety of standard signal levels. In addition, many of the PLL devices are spread-spectrum clock (SSC) compatible. There is also a selection of clock drivers for memory applications.

Applications Support

Do you need help selecting the timing devices for your board designs? Are you concerned about jitter, skew, zero delay and other parameters affecting your timing budget? The TI technical application support team will work with you on TI's clock and timing products and provide solution options for your board-level concerns. To get answers to your technical questions, contact your nearest TI Product Information Center listed at the end of this guide or select from the TI Worldwide options at: http://clocks.ti.com

Overview

Clock Generation and Distribution Circuits

Non-PLL Clock Buffers— TI offers both single-ended and differential clock buffers that perform from below 200 MHz up to 3.5 GHz in a variety of fanout options. In addition to simple buffering, TI also offers a mixed-signal option for customers needing differential signals (LVPECL/LVDS) and single-ended signals (LVTTL/LVCMOS) from the same device.

PLL Clock Buffers — TI offers zero-delay buffers that provide single-ended PLL functions for general-purpose applications and differential PLL functions for DDR clocking.

Clock Generators/Synthesizers — TI offers programmable clock generators with 0 ppm offset that can produce an almost independent output frequency from a given input frequency.

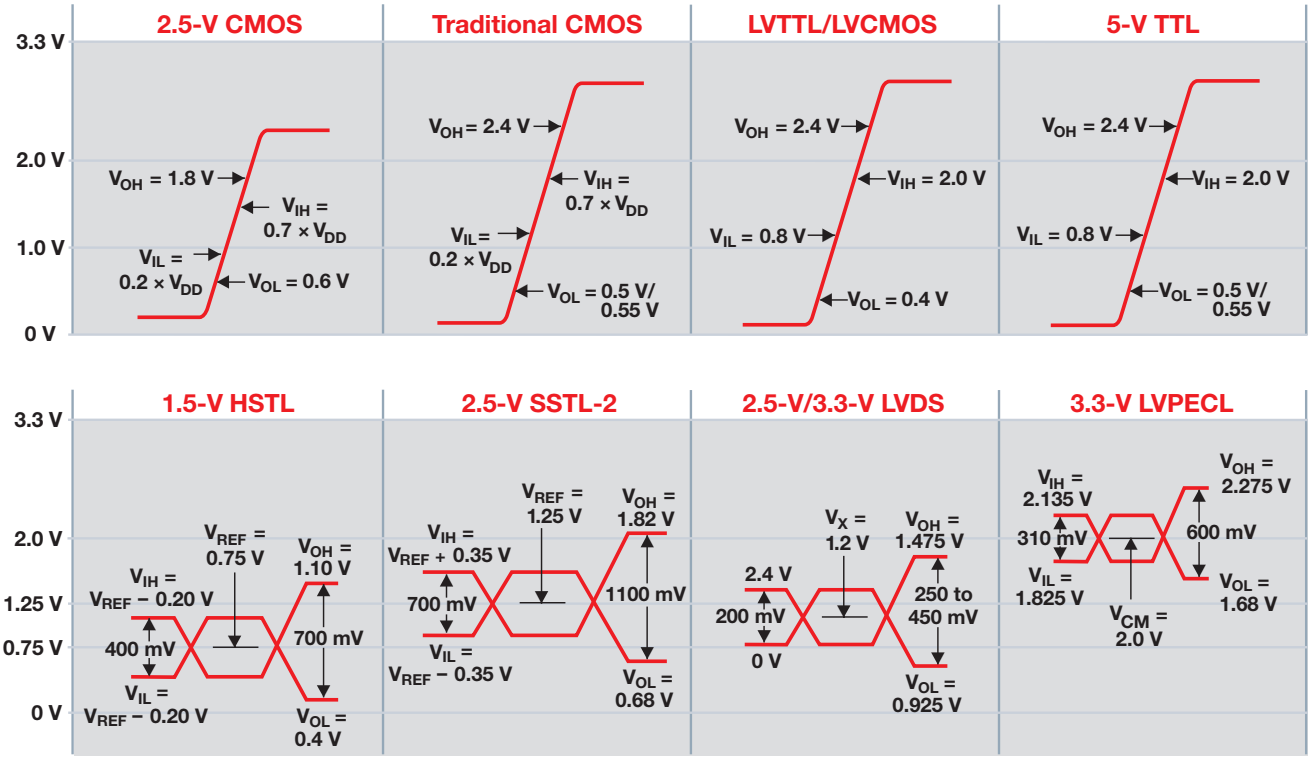
Femto-Second Precision Clock Generators/ Synthesizers/Jitter Cleaners —TI offers low-noise clock synthesizers with jitter cleaning that is fully integrated or with external VCXO/VCO

Oscillator ICs —TI offers both PLL and non-PLL oscillator ICs that accept input from crystal.

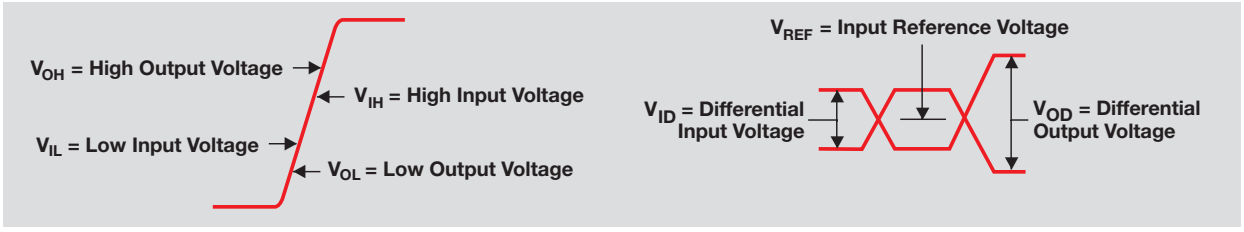
Memory PLLs/Registers —TI offers zero-delay PLLs and registers that target DDR, DDR2 and DDR3 memory standards as well as Rambus® and XDR™ clock generators.

RF PLLs —TI offers a family of low-noise RF frequency synthesizers (PLLs) with output frequencies of up to 2.4 GHz. Devices offer hardware/software power-down modes and optionally integrated on-chip VCO. These devices have small packages and a simple 3-wire interface for ease of programming. Target applications are: wireless infrastructure, portable wireless, wireless LAN, wireless transceivers and communication test equipment.

Signal-level comparisons

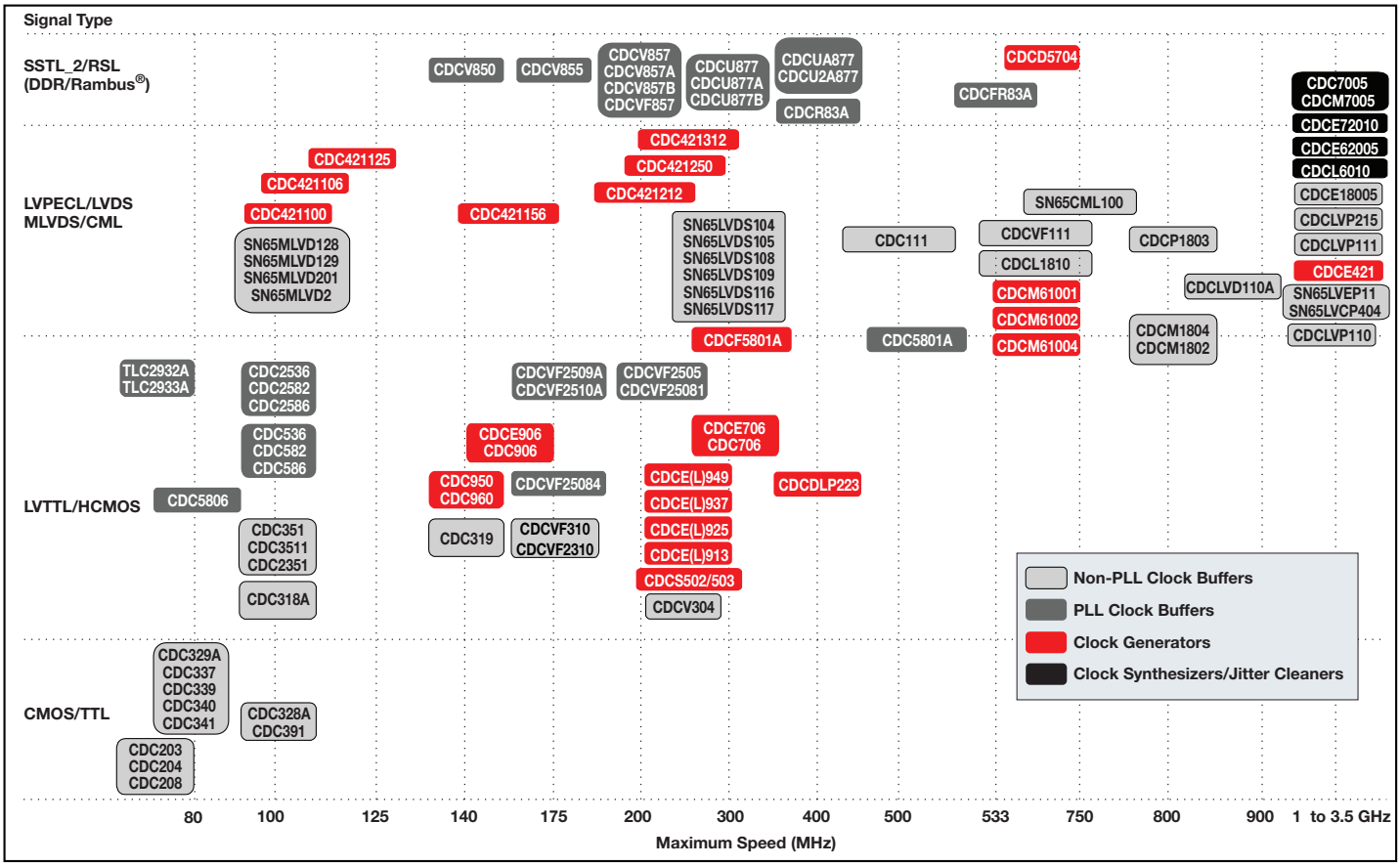


Signal-level definitions

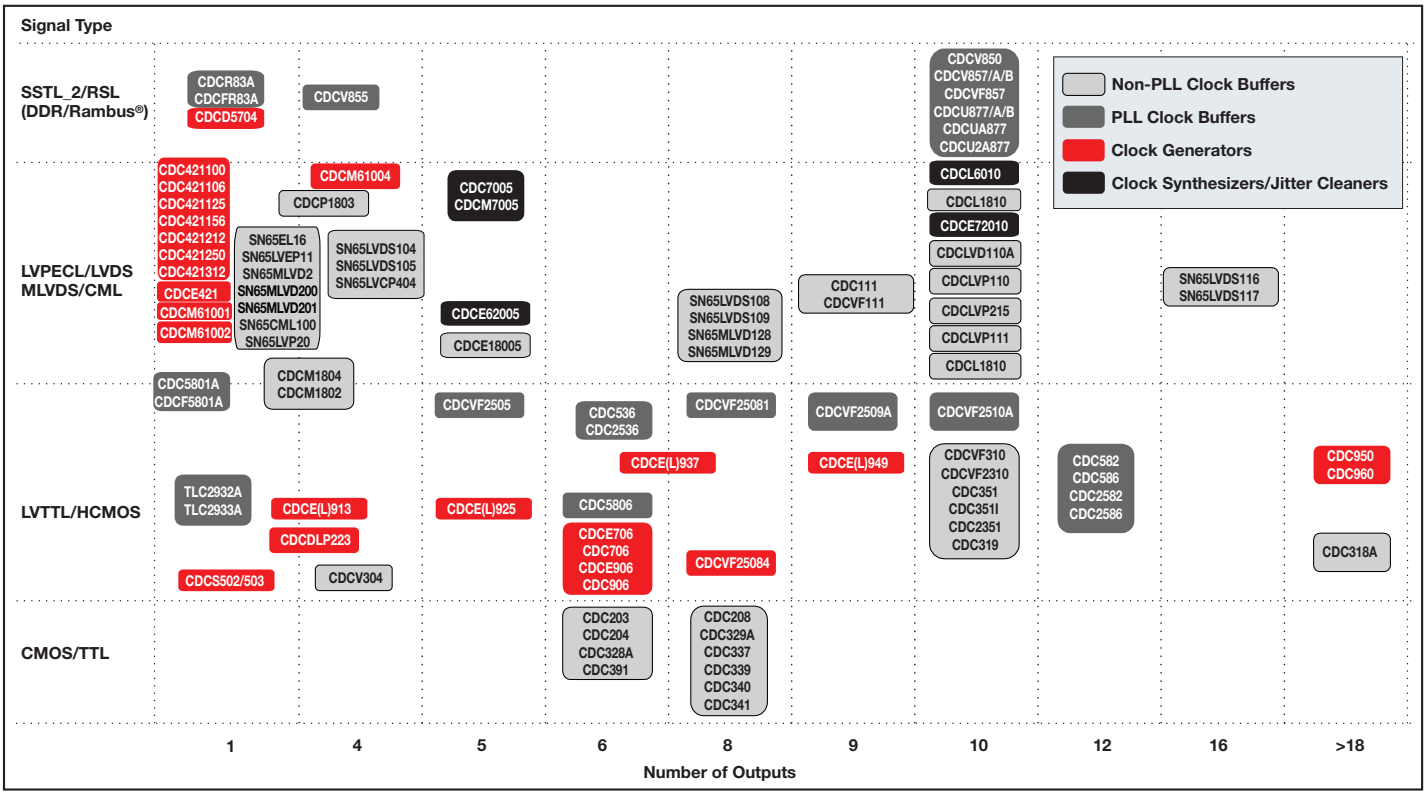


Overview

Clock Selection by Maximum Speed and Signaling Type



Clock Selection by Number of Outputs and Signaling Type



1:5 LVPECL/LVDS/LVCMOS Mixed Mode Buffer with EEPROM

CDCE18005

Get samples, datasheets and evaluation modules at: **www.ti.com/sc/device/CDCE18005**

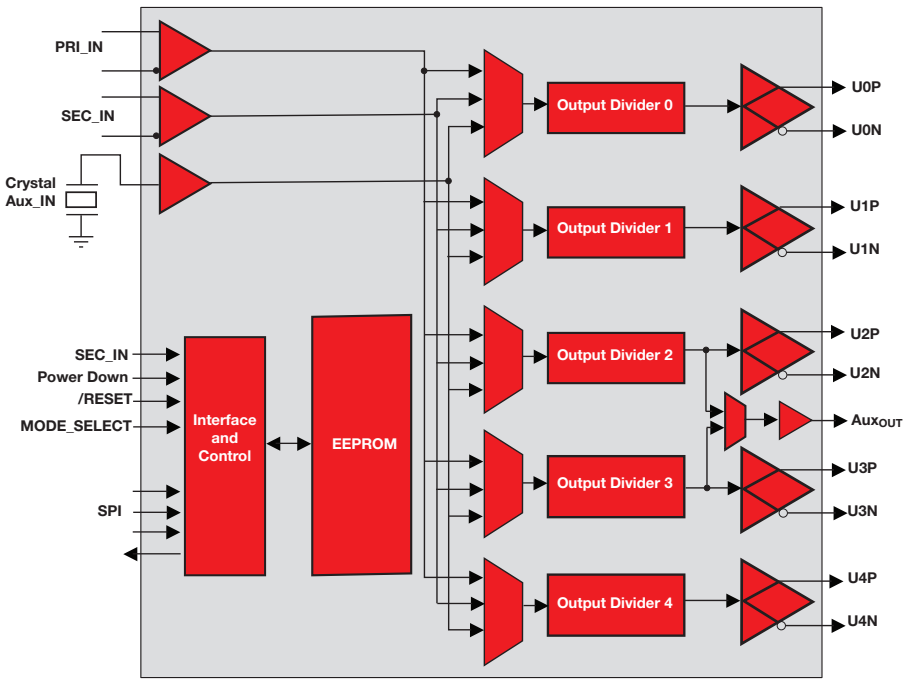
CDCE18005 is a high performance low additive jitter clock buffer with five programmable output buffers. Each output can be configured to be LVPECL, LVDS or two LVCMOS. The output frequency is proportional to the frequency of the input and the output divider. Each output has an independent output divider and each output can be sourced from the primary input, secondary input, auxiliary or smart mux output. All device settings are programmable through a SPI serial interface. The device operates in 3.3-V supply environment and is characterized for operation from –40°C to +85°C.

Key Features

- Five universal outputs that can be programmed to be up to 5 LVPECL, 5 LVDS or 10 LVCMOS output buffers or any combination
- Two high-speed clock inputs (primary and secondary)
- Third auxiliary input that can accept a crystal from 2 MHz to 42 MHz or an LVCMOS input up to 100 MHz
- In full fanout buffer mode (divide by one), it can operate up to 1.5 GHz in LVPECL, 800 MHz in LVDS or 200 MHz in LVCMOS mode
- In fanout buffer mode (using the output divider) it can operate up to 1.175 GHz in LVPECL, 800 MHz in LVDS or 200 MHz in LVCMOS mode
- Additive jitter as low as 80-fs RMS (integrated from 10 KHz to 20 MHz)
- Output divider is selectable to divide by 1, 2, 3, 4, 5, 6, 8, 10, 12, 16, 18, 20, 24, 28, 30, 32, 36, 40, 42, 48, 50, 56, 60, 64, 70 and 80 on each output individually with skew control
- Independent coarse skew control for all outputs
- Power consumption 1 W in typical application at 3.3-V supply
- Integrated on-chip non-volatile memory (EEPROM) to store settings without the need to apply high voltage to the device
- ESD protection exceeds 2-kV HBM

Applications

- Low-jitter clock driver for high-end wireless and datacom applications
- Clock generation from a crystal input or a reference input



CDCE18005 functional diagram.

1:10 LVPECL Buffer with Input Mux

CDCLVP111

Get samples and datasheets at: **www.ti.com/sc/device/CDCLVP111**

The CDCLVP111 clock driver distributes one differential clock pair of LVPECL input to ten pairs of differential LVPECL clock outputs with minimum skew for clock distribution. The CDCLVP111 can accept two clock sources into an input multiplexer. The CDCLVP111 is specifically designed for driving 50-Ω transmission lines.

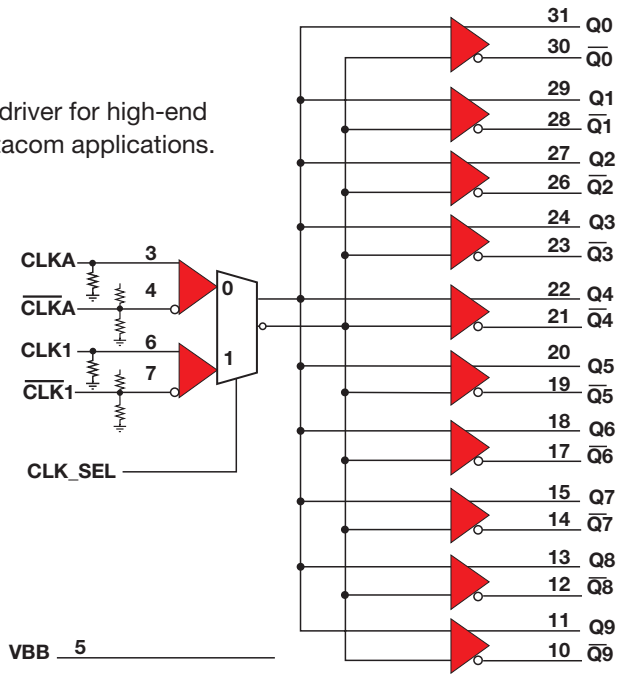
Key Features

- Single supply voltage required, 3.3-V or 2.5-V supply
- Selectable clock input through CLK_SEL
- Low-output skew (typ 15 ps)
- Additive jitter less than 1 ps
- Propagation delay less than 350 ps
- Open input default state
- LVDS, CML, SSTL input compatible
- Frequency range from DC to 3.5 GHz
- Packaging: 32-pin LQFP and QFN

- Pin-to-pin compatible with MC100 series EP111, ES6111, LVEP111, PTN1111

Applications

- Low-jitter clock driver for high-end wireless and datacom applications.



CDCLVP111 functional diagram.

Dual 1:5 LVPECL Buffer

CDCLVP215

Get samples and datasheets at: **www.ti.com/sc/device/CDCLVP215**

The CDCLVP215 clock driver distributes 2× one differential clock pair of LVPECL to 5 pairs of differential LVPECL clock outputs with minimum skew. The CDCLVP215 is specifically designed for driving 50-Ω transmission lines up to 3.5 GHz. The CDCLVP215 is characterized for operation from –40°C to 85°C.

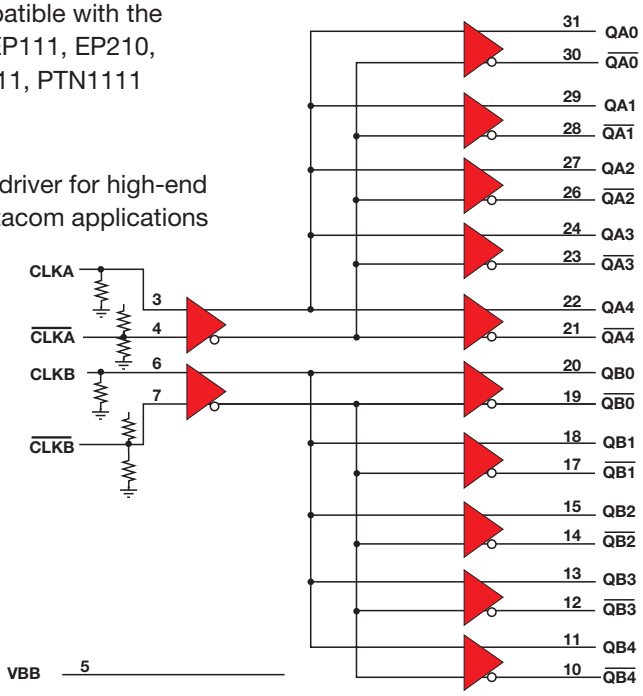
Key Features

- Supports a wide supply-voltage range from 2.375 V to 3.8 V
- Low-output skew (typ 15 ps) for clock-distribution applications
- VBB reference voltage output for single-ended clocking
- Frequency range from DC to 3.5 GHz
- Packaging: QFN32

- Pin-to-pin compatible with the MC100 Series EP111, EP210, ES6111, LVEP111, PTN1111

Applications

- Low-jitter clock driver for high-end wireless and datacom applications



CDCLVP215 functional diagram.

1:10 LVDS Buffer up to 900 MHz

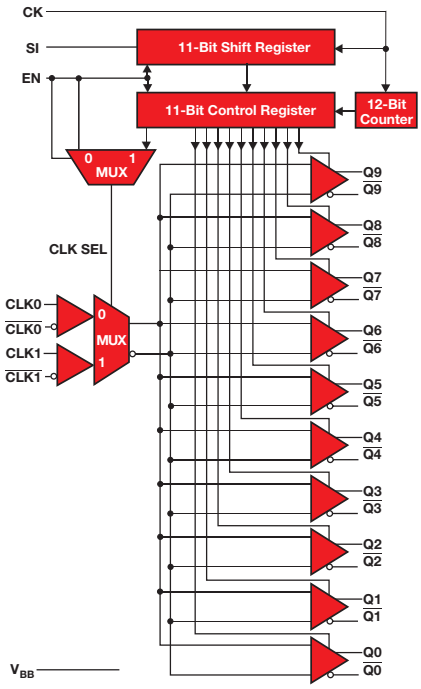
CDCLVD110A

Get samples and datasheets at: **www.ti.com/sc/device/CDCLVD110A**

The CDCLVD110A clock driver distributes one pair of differential LVDS clock inputs (either CLK0 or CLK1) to 10 pairs of differential clock outputs (Q0, Q9) with minimum skew for clock distribution. The CDCLVD110A is specifically designed for driving 50-W transmission lines. When the control enable is high (EN = 1), the 10 differential outputs are programmable in that each output can be individually enabled/disabled (3-stated) according to the first 10 bits loaded into the shift register.

Key Features

- Low-output (<30-ps typical) skew for clock-distribution applications
- Distributes one differential clock input to 10 LVDS differential clock outputs
- Typical signaling rate capability of up to 1.1 GHz
- Configurable register (SI/CK) individually enables/disables outputs; selectable CLK0, CLK0 or CLK1, CLK1 inputs
- Full rail-to-rail common-mode input range
- Receiver input threshold = ±100 mV
- Fail-safe I/O pins for VDD = 0 V (power down)
- Packaging: 32-pin TQFP (9 x 9 mm)



CDCLVD110A functional diagram.

LVPECL/LVCMOS Buffer

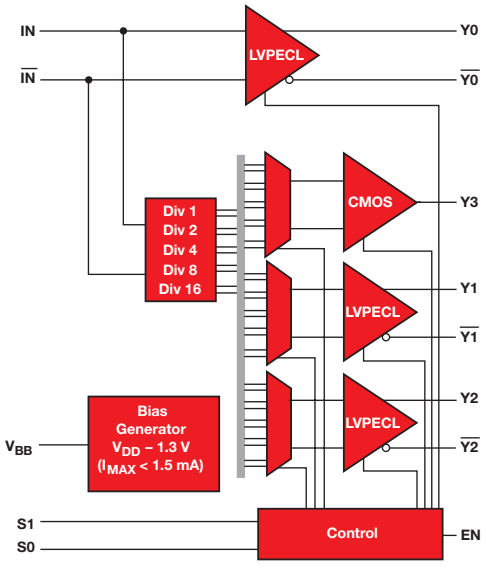
CDCM1804

Get samples and datasheets at: **www.ti.com/sc/device/CDCM1804**

The CDCM1804 clock driver distributes one pair of differential clock inputs to three pairs of LVPECL differential clock outputs, with minimum skew for clock distribution. It is specifically designed for driving 50-W transmission lines. Additionally, the CDCM1804 offers a single-ended LVCMOS output. This output is delayed by 1 ns over the three PECL output stages to minimize noise impact during signal transitions.

Key Features

- Distributes one differential clock input to three LVPECL differential clock outputs and offers one LVCMOS single-ended output
- Programmable output divider for two LVPECL outputs and one LVCMOS output
- Low-output (20-ps typical) skew for clock distribution applications for LVEPCL outputs; 1-ns output skew between LVCMOS and LVPECL transitions, minimizing noise
- VCC range: 3.0 to 3.6 V
- Signaling rate of up to 800 MHz for LVPECL and 200 MHz for LVCMOS
- Differential input stage for very wide common-mode range also provides VBB bias-voltage output for single-ended input signals
- Receiver input threshold: ±75 mV
- Packaging: 24-pin MLF (4 x 4 mm)



CDCM1804 functional diagram.

Differential and Single-Ended Output in One Buffer

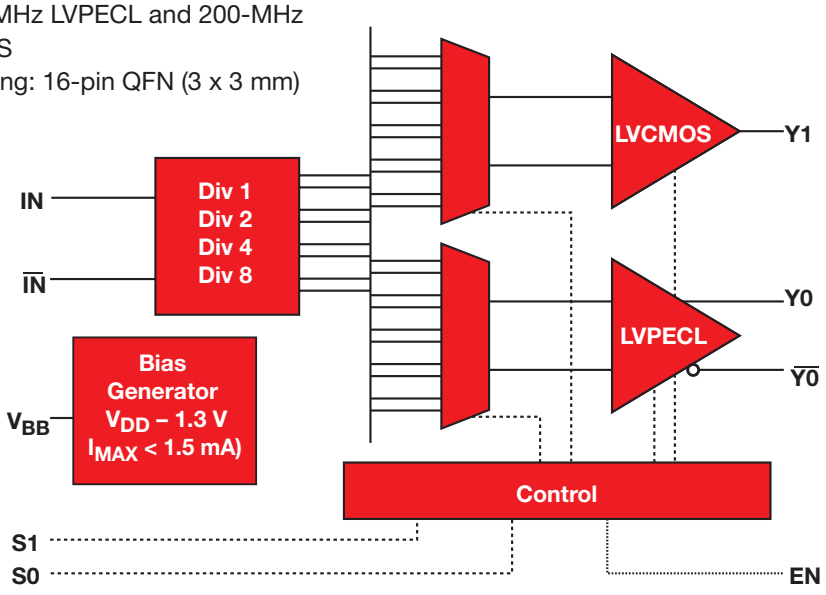
CDCM1802

Get samples, datasheets and app reports at: **www.ti.com/sc/device/CDCM1802**

The CDCM1802 clock driver distributes one pair of differential clock inputs to one pair of LVPECL differential clock outputs and to one single-ended LVCMOS output. The LVCMOS output is delayed by 1.6 ns over the PECL output stage to minimize noise impact during signal transitions.

Key Features

- Distributes one differential clock input to one LVPECL differential clock output and to one LVCMOS single-ended output
- Programmable output divider for both LVPECL and LVCMOS outputs
- 1.6-ns output skew between LVCMOS and LVPECL transitions, minimizing noise
- 3.3-V power supply (2.5-V functional); signaling rate of up to 800-MHz LVPECL and 200-MHz LVCMOS
- Packaging: 16-pin QFN (3 x 3 mm)



CDCM1802 functional diagram.

1.8-V, 10-Output High-Performance Clock Buffer

CDCL1810

Get samples and datasheets at: **www.ti.com/sc/device/CDCL1810**

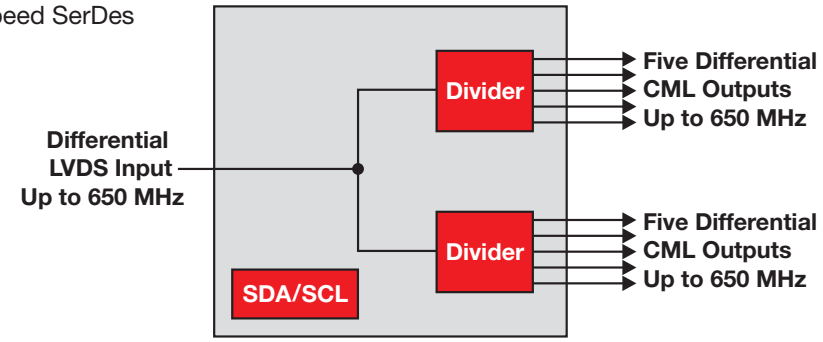
The CDCL1810 is a high-performance clock distributor with built-in dividers and phase adjustment. The device operates with a 1.8-V supply to save power and includes 10 outputs that can operate at up to 650 MHz.

Key Features

- Additive jitter <300 fS rms (design target)
- Low-voltage differential signaling (LVDS) input, 100-W differential on-chip termination, up to 650 MHz
- Differential current-mode logic (CML) outputs, 50-W single-ended on-chip termination, up to 650 MHz
- Two groups of five outputs each with independent frequency division ratios
- Output frequency is derived from input frequency divided by 1, 2, 4, 5, 8, 10, 16, 32, 40
- Jitter cleaning of SerDes reference clocks for 1/10 gigabit ethernet, 1x/2x/4x/10x fibre channel, PCI Express, serial ATA, SONET, CPRI, OBSAI
- Up to 1:11 clock buffering and fanout

Applications

- Low-jitter clocking for high-speed SerDes



CDCL1810 functional diagram.

2.5V/3.3V 3GHz 1:2 PECL/ECL Fanout Buffer

SN65LVEP11

Get samples and datasheets at: **www.ti.com/sc/device/SN65LVEP11**

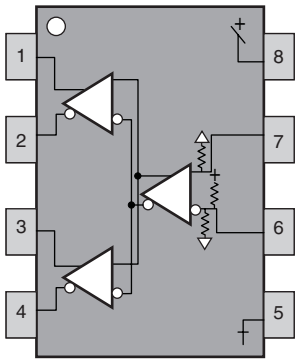
The SN65LVEP11 is a differential 1:2 PECL/ECL fanout buffer. The device includes circuitry to maintain known logic levels when the inputs are in an open condition. Single-ended clock input operation is limited to V_{CC} ≥ 3.0 V in PECL mode or V_{EE} ≤ 3.0 V in NECL mode. The device can be powered with 2.5 V and 3.3 V supplies. SOIC and MSOP packages are available.
Other devices in the family include 3.3-V and 5-V powered buffers and ECL/TTL translators in a variety of frequencies. Please consult the table below.

Key Features

- 1:2 PECL/ECL fanout buffer
- Operating range
  - PECL: V_{CC} = 2.375 V to 3.8 V with V_{EE} = 0 V
  - NECL: V-1 pt = 0 V with V_{EE} = –2.375 V to –3.8 V
- Support for clock frequencies 3.0 GHz
- Drop in compatible to MC100LVEP11 and SY100LVEP11

Applications

- Clock and data splitter and buffer
- Telecom, test, medical



SN65LVEP11 block diagram.

Part Number	Supply Voltage	Function	Frequencies
SN65EL11	5	1:2 Splitter	2.5GHz
SN65EL16	5	1:1 Buffer	2GHz
SN65ELT20	5	TTL/PECL	430MHz
SN65ELT22	5	Dual TTL/PECL	490MHz
SN65EPT22	3.3	Dual TTL/PECL	2GHz
SN65LVEL11	3.3	1:2 Splitter	2GHz
SN65LVELT22	3.3	Dual TTL/PECL	1.75GHz
SN65LVEP11	2.5/3.3	1:2 Splitter	3GHz

3.3-V PLL Clock Driver with Power-Down Mode

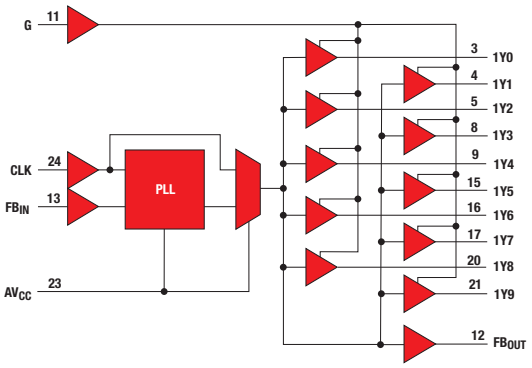
CDCVF2510A

Get samples, datasheets and app reports at: **www.ti.com/sc/device/CDCVF2510A**

The CDCVF2510A is specifically designed for use with synchronous DRAMs. One bank of 10 outputs provides 10 low-skew, low-jitter copies of CLK. Outputs are enabled or disabled via the control (G) input. When the G input is high, the outputs switch in phase and frequency with CLK; when the G input is low, the outputs are disabled to the logic-low state. The device automatically goes into power-down mode when no input signal (<1 MHz) is applied to CLK.

Key Features

- Meets and exceeds PC133 SDRAM registered DIMM specification Rev. 1.1
- Spread-spectrum-clock compatible
- Operating frequency: 20 to 175 MHz
- Static phase error distribution of ±125 ps at 66 to 166 MHz
- |70|-ps cycle-to-cycle jitter at 66 to 166 MHz
- Auto frequency detection to disable device (power-down mode)
- Distributes one clock input to one bank of 10 outputs
- External feedback (FBIN) terminal is used to synchronize the outputs to the clock input
- 25-W on-chip series damping resistors OBSAI
- No external RC network required
- Packaging: 24-pin TSSOP (7.8 x 6.4 mm)



CDCVF2510A functional diagram.

Low-Jitter Clock Multiplier/Divider with Programmable Delay and Phase Alignment

CDCF5801A

Get samples, datasheets, evaluation modules and app reports at: **www.ti.com/sc/device/CDCF5801A**

The CDCF5801A provides clock multiplication and division from a reference clock (REFCLK) signal. It also allows delay or advance of the CLKOUT/CLKOUTB with steps of 2.6 mUI through a unique phase aligner

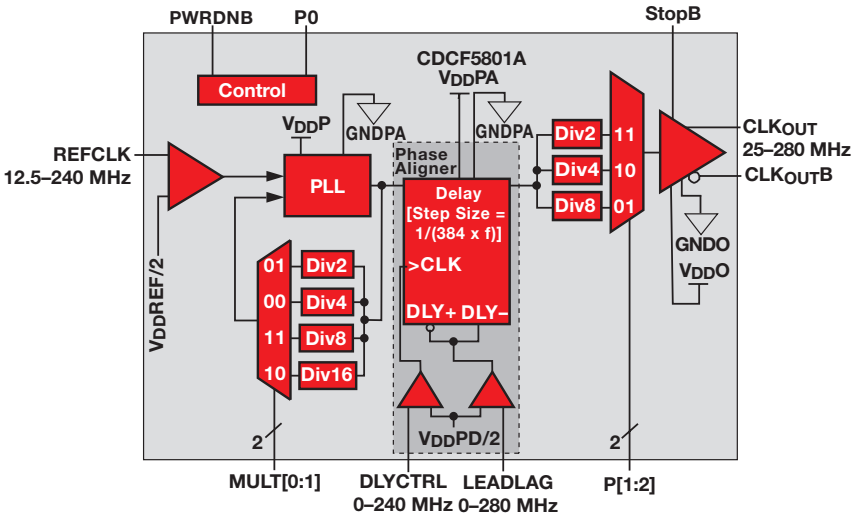
- Industrial temperature range: –40°C to 85°C

Applications

- Phase adjustment
- Low-jitter multiplier
- Low-jitter divider

Key Features

- Low-jitter clock multiplier x1, x2, x4 or x8:
  - Input frequency: 12.5 to 240 MHz
  - Output frequency: 25 to 280 MHz
- 2.6-mUI programmable bidirectional delay steps
- One single-ended input and one differential output pair (input tolerates LVPECL and LVTTL)
- Output can drive LVPECL, LVDS and LVTTL
- Spread-spectrum-clock tracking ability to reduce EMI



CDCF5801A functional diagram.

4/3/2/1-PLL Clock Synthesizer with 3.3-V/2.5-V/1.8-V I/Os and EEPROM

CDCE949 family

Get samples, datasheets, evaluation modules and app reports at: **www.ti.com/sc/device/CDCE949** or **www.ti.com/sc/device/CDCEL949**

The CDCE949 and CDCEL949 are modular PLL-based programmable clock synthesizers. They generate up to nine output clocks from a single input frequency. Each output can be programmed for any clock frequency up to 230 MHz, using up to four independent configurable PLLs.

The input accepts an external crystal or LVCMOS clock signal. If an external crystal is used, an on-chip load capacitor is adequate for most applications. Additionally, an on-chip VCXO is selectable, allowing synchronization of the output frequency to an external control signal. The deep M/N divider ratio allows the generation of zero-ppm audio/video, networking (WLAN, *BlueTooth*®, ethernet, GPS) or interface (USB, IEEE1394, Memory Stick) clocks from a reference input frequency, such as 27 MHz. All PLLs support spread-spectrum clocking (SSC). SSC can be center-spread or down-spread clocking. Based on the PLL frequency and the divider settings, the internal loop-filter components are automatically adjusted to achieve high stability, and to optimize the jitter-transfer characteristics of each PLL.

The device supports non-volatile EEPROM programming for easy customization of the device to the application. All device settings are programmable through the SDA/SCL bus, a 2-wire serial interface.

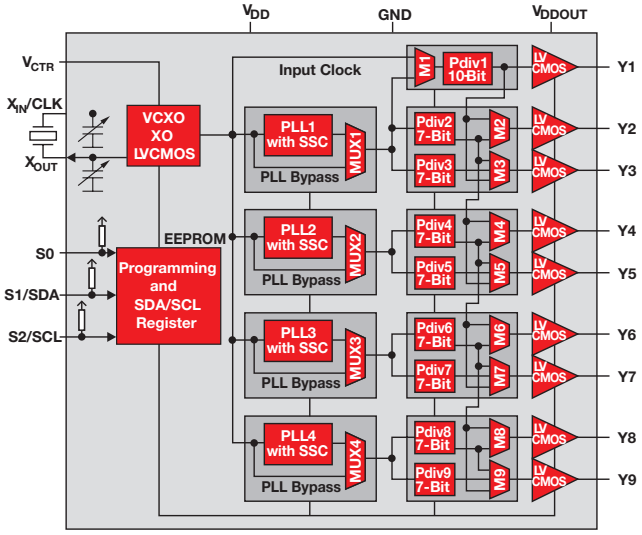
The CDCx949 operates with 1.8-V core supply and has separate output supply pins, VDDOUT, 1.8 V for the CDCEL949, and 2.5 V to 3.3 V for CDCE949.

Applications

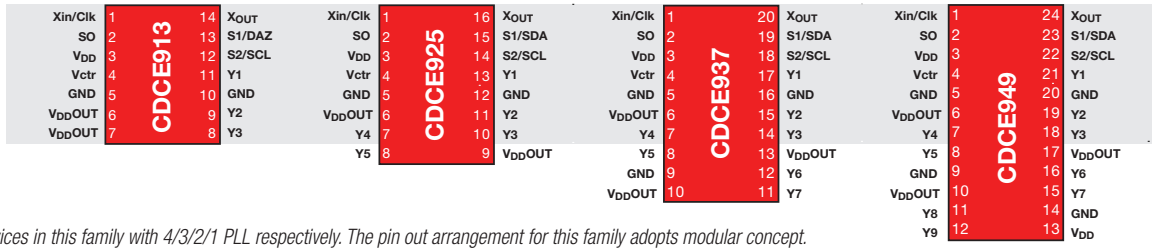
- Digital media systems (audio/video), IPSTB/
- TV/phone, streaming media (DVD-P/R), GPS
- Receivers, portable media, printers, TI DSP, OMAP™ and DaVinci™ media processors

Key Features

- VCXO input with ±150ppm pulling range
- Nine low-jitter, low-skew outputs
- Three user definable control inputs
- Spread spectrum clocking
- In-system, hot-programmable by SDA/SCL
- On-chip EEPROM
- 1.8-V supply voltage, 3.3-V or 2.5-V I/O for CDCE949 and 1.8-V I/O for CDCEL949
- –40°C to 85°C temperature range
- Packaging: 24-pin TSSOP



CDCE(L)949 functional diagram.



There are eight devices in this family with 4/3/2/1 PLL respectively. The pin out arrangement for this family adopts modular concept.

Device	CDCE949	CDCE937	CDCE925	CDCE913	CDCEL949	CDCEL937	CDCEL925	CDCEL913
Supply Voltage (V)	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8
I/O Voltage (V)	3.3/2.5	3.3/2.5	3.3/2.5	3.3/2.5	1.8	1.8	1.8	1.8
Number of PLL	4	3	2	1	4	3	2	1
Number of Outputs	9	7	5	3	9	7	5	3
Pins (TSSOP)	24	20	16	14	24	20	16	14
Price[1]	2.20	2.00	1.80	1.60	2.20	2.00	1.80	1.60

[1] *Suggested resale price in U.S. dollars in quantities of 1,000.*

Spread Spectrum Driver/Multiplier

CDCS502, CDCS503

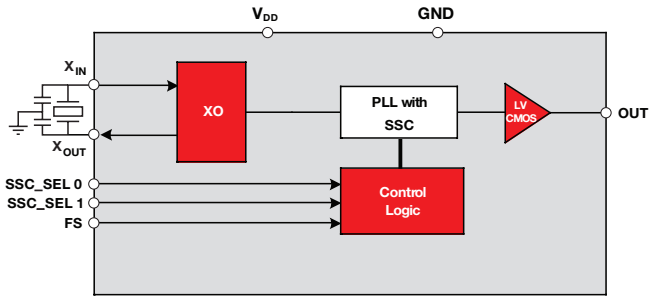
Get samples and datasheets at: **www.ti.com/sc/device/CDCS502** or **www.ti.com/sc/device/CDCS503**

The CDCS502 and CDCS503 are spread-spectrum-capable clock multipliers with selectable frequency multiplication. The CDCS502 device accepts a crystal signal at the input and it features an advanced gain controlled fundamental mode crystal oscillator stage that excepts crystals from 8 MHz to 32 MHz with an ESR of up to 100 Ω and a maximum power dissipation as low as 50 µW. The CDCS503 device accepts a 3.3-V LVCMOS signal at the input.

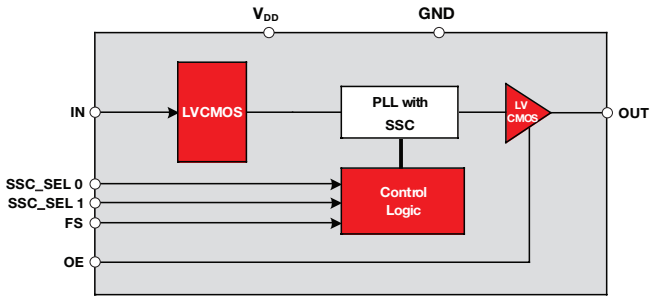
The input signal is then processed by a PLL, capable of spreading the clock signal up to 2% and also multiplying the frequency by the factor of 4. By this, the device can generate output frequencies between 8 MHz and 108 MHz with or without SSC.

Key Features

- Crystal oscillator with selectable output frequency and selectable SSC
- SSC controllable via 2 external pins
- Frequency multiplication selectable between x1 or x4 with one external control pin
- Output disable via control pin
- Single 3.3-V device power supply
- Wide temperature range: – 40°C to 85°C
- Packaging: 8-pin TSSOP



CDCS502 block diagram.



CDCS503 block diagram.

Programmable 3-PLL Clock Synthesizer/Multiplier/Divider

CDCE906

Get samples, datasheets, evaluation modules and app reports at: **www.ti.com/sc/device/CDCE906**

The CDCE906 is optimized for consumer applications. It generates precise video (27 or 54 MHz) and audio system clocks from multiple sampling frequencies (fS = 16, 22.05, 24, 32, 44.1, 48, 96 kHz).

Key Features

- Accepts LVCMOS or differential input frequencies of up to 167 MHz
- Six LVCMOS outputs with output frequencies of up to 167 MHz
- Commercial temperature range: 0°C to 70°C
- Packaging: 20-pin TSSOP (6.5 x 6.4 mm)

Programmable 3-PLL Clock Synthesizer/Multiplier/Divider

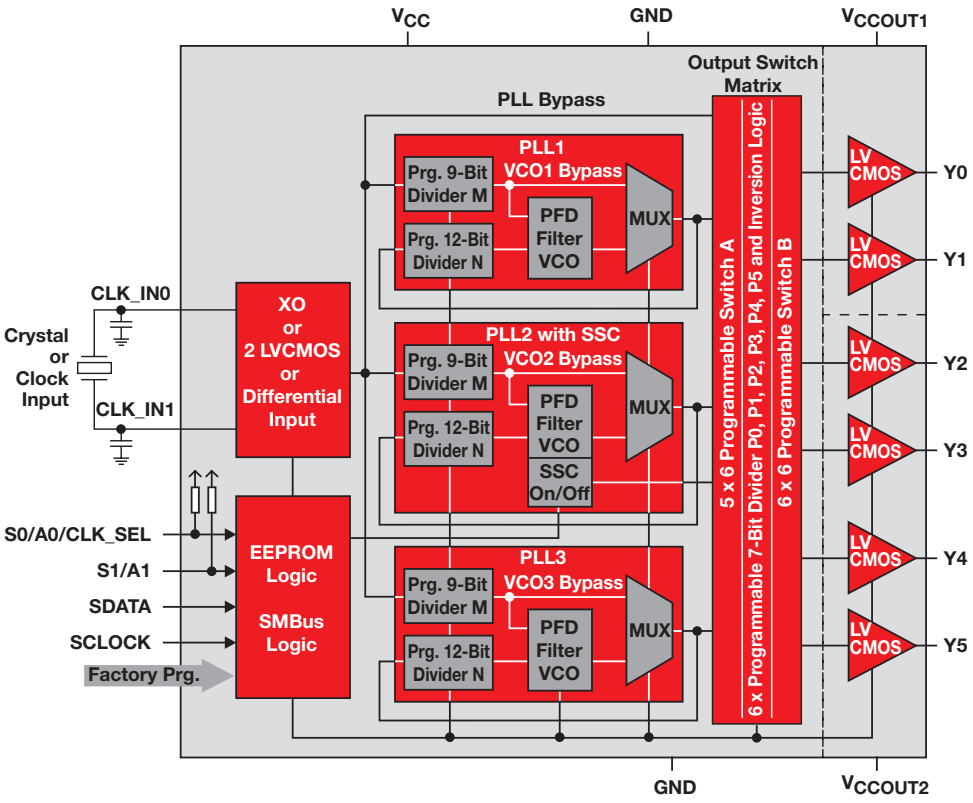
CDCE706

Get samples, datasheets, evaluation modules and app reports at: **www.ti.com/sc/device/CDCE706**

The CDCE706 can produce an almost independent output frequency from a given input frequency. Input frequency can be derived from an LVCMOS, a differential input clock or a single crystal. To achieve an independent output frequency for each PLL, the reference divider M can be set to values ranging from 1 to 511 and the feedback divider N from 1 to 4095. The CDCE706 includes three PLLs; of those, one can support a spread-spectrum clock (SSC). PLL1, PLL2 and PLL3 are designed for frequencies up to 300 MHz and are optimized for 0-ppm applications with wide divider factors.

Key Features

- User-programmable PLL frequencies
- EEPROM programming without the need to apply high programming voltage
- Easy in-circuit programming via SMBus data interface
- Wide PLL divider ratio allows 0-ppm output clock error
- Accepts crystal frequencies from 8 MHz up to 54 MHz
- Accepts LVCMOS or differential input frequencies of up to 200 MHz
- Two programmable control inputs (S0/S1, A0/A1) for user-defined control signals
- Six LVCMOS outputs with output frequencies up to 300 MHz
- Free selectable output frequency via programmable output switching matrix (6 x 6) including 7-bit post-divider for each output
- Low period jitter (60 ps typical)
- Features SSC for lowering system EMI
- Programmable output slew-rate control (SRC) for lowering system EMI
- 3.3-V device power supply
- Industrial temperature range: –40°C to 85°C
- Development and programming kit for easy PLL design and programming (TI's ClockPro™)
- Packaging: 20-pin TSSOP (6.5 x 6.4 mm)



CDCE706/ CDCE906 functional diagram.

Ultra-Low-Jitter Xtal Clock Generator

CDCM61001/002/004

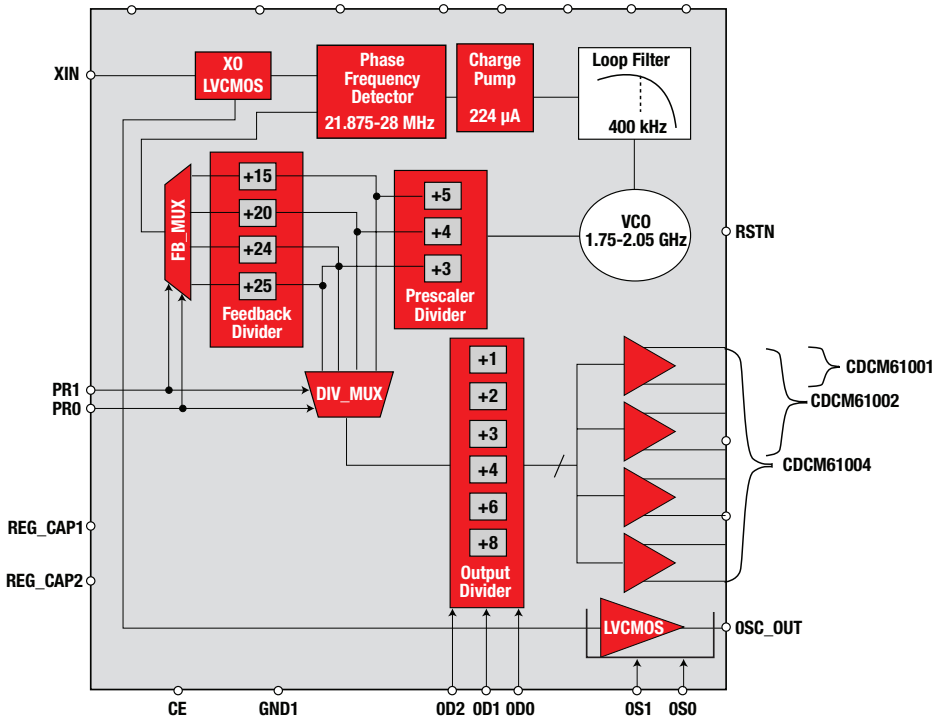
Get samples, datasheets and evaluation modules at: **www.ti.com/sc/device/CDCM61001**, **CDCM61002**, or **CDCM61004**

The CDCM61001/002/004 are highly versatile, low-jitter frequency generators which can generate one/two/four low-jitter clock outputs, selectable among LVPECL, LVDS or LVCMOS, from a low-frequency crystal or LVCMOS input for a variety of wireline and data-communication applications. The CDCM6100x features an on-chip PLL that can be easily configured solely through control pins. The overall output jitter performance is less than 1ps, RMS or 35ps, pk-pk thus making the device a perfect choice for use in demanding applications like SONET, ethernet, fibre channel, and SAN. The CDCM6100x is packaged in a small 32-pin 5mm x 5mm QFN package.

- Output duty cycle is corrected to 50% (±5%)
- Low output skew of 30 ps on LVPECL outputs
- Divider Programming using Control Pins (2 pins for prescaler/feedback divider, 3 pins for output divider and 2 pin for output select)
  OSC_OUT pin provides access to measure input Xtal frequency
- 3.3-V core and I/O power supply
- Industrial temperature range – 40°C to 85°C
- ESD protection exceeds 2-kV HBM
- Packaging: 32-pin QFN (RHB)

Key Features

- Input frequency range is 21.875 MHz to 28.47 MHz, takes one single ended or crystal reference input including 24.8832 MHz, 25 MHz and 26.5625 MHz
- Output frequencies in MHz include: 62.5, 74.25, 75, 77.76, 100, 106.25, 125, 150, 155.52, 156.25, 159.375, 187.5, 200, 212.5, 250, 311.04, 312.5, 622.08, 625
- On-chip VCO operate in the frequency region of 1.75 GHz to 2.05 GHz
- 4x output is available, pin selectable between LVPECL, LVDS or 2 LVCMOS and operate at 3.3 V
- Output frequency is selectable by /1, /2, /3, /4, /6, /8 from a single output divider
- Fully integrated PLL loop Bandwidth of 400 kHz
- Very low phase-noise PLL core with <–148 dBc/Hz at offset of 5 MHz, total jitter < 1 ps, RMS (10 kHz-20 MHz) or < 35 ps, pk-pk total period jitter at 625-MHz LVPECL outputs



CDCM6100x functional block diagram.

10 Output Clock Synchronizer and Jitter Cleaner with External VC(X)O

CDCE72010

Get samples, datasheets, evaluation modules and app reports at: **www.ti.com/sc/device/CDCE72010**

The CDCE72010 is a low-phase-noise and low-skew clock synchronizer that synchronizes a voltage controlled crystal oscillator (VCXO) or voltage controlled oscillator (VCO) frequency to one of the two reference clocks. The programmable pre-dividers M and reference divider and the feedback-dividers N and P give a high flexibility to the frequency ratio of the reference clock to VC(X)O. The PLL loop bandwidth and damping factor can be adjusted to meet different system requirements. The outputs of CDCE72010 are user definable and can be any combination of up to 10 LVPECL/ LVDS outputs or up to 20 LVCMOS. The CDCE72010 supports frequency hold-over mode and fast-frequency-locking for fails-safe and increased system redundancy. All device settings, like outputs signaling, divider value, input selection, and many more, are programmable by SPI (4-wire serial peripheral interface). The device is in a QFN-64 package, operates in a 3.3-V environment, and is characterized for operation from –40°C to +85°C.

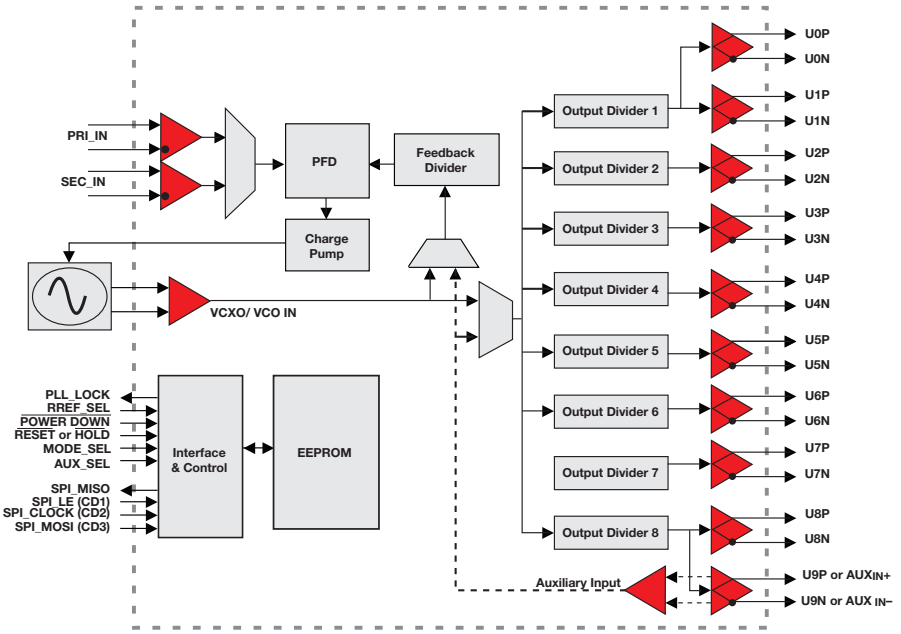
The CDCE72010 is designed to drive high-performance data converters (used in applications such as wireless base station transceiver cards, medical equipment and test equipment) where ultra-low jitter performance is critical. It is the recommended clock solution for TI high speed ADCs such as ADS54xx, ADS6xxx, ADS3xxx and high-speed DACs such as DAC568X.

Key Features

- Outputs can be 10 LVPECL or 10 LVDS or 20 LVCMOS or any combination up to 1.5 GHz
- Output divider is selectable to divide by 1, 2, 3, 4, 5, 6, 8, 10, 12, 16, 18, 20, 24, 28, 30, 32, 36, 40, 42, 48, 50, 56, 60, 64, 70 and 80 on each output individually up to eight dividers. (except for output 0 & 9. output 0 follows Output 1 divider and output 9 follows output 8 divider.)
- Accepts two differential Inputs (LVPECL or LVDS) up to 500 MHz (or two LVCMOS inputs up to 250 MHz) as PLL reference
- VCXO_IN frequencies up to 1.5 GHz (LVPECL) , 800 MHz for (LVDS) and 250 MHz for LVCMOS level signaling
- Output 9 can be converted to an auxiliary input as a second VC(X)O or to serve as PLL feedback signal
- Optional configuration default pins to select between two default settings stored in EEPROM.
- SPI controllable device settings

Applications

- Wireless BTS (macro, micro cells)
- High-end medical systems
- Telecommunications
- Test equipment



CDCE72010 high-level block diagram.

Low-Phase-Noise Clock Synthesizer/Multiplier/Divider/Jitter Cleaner

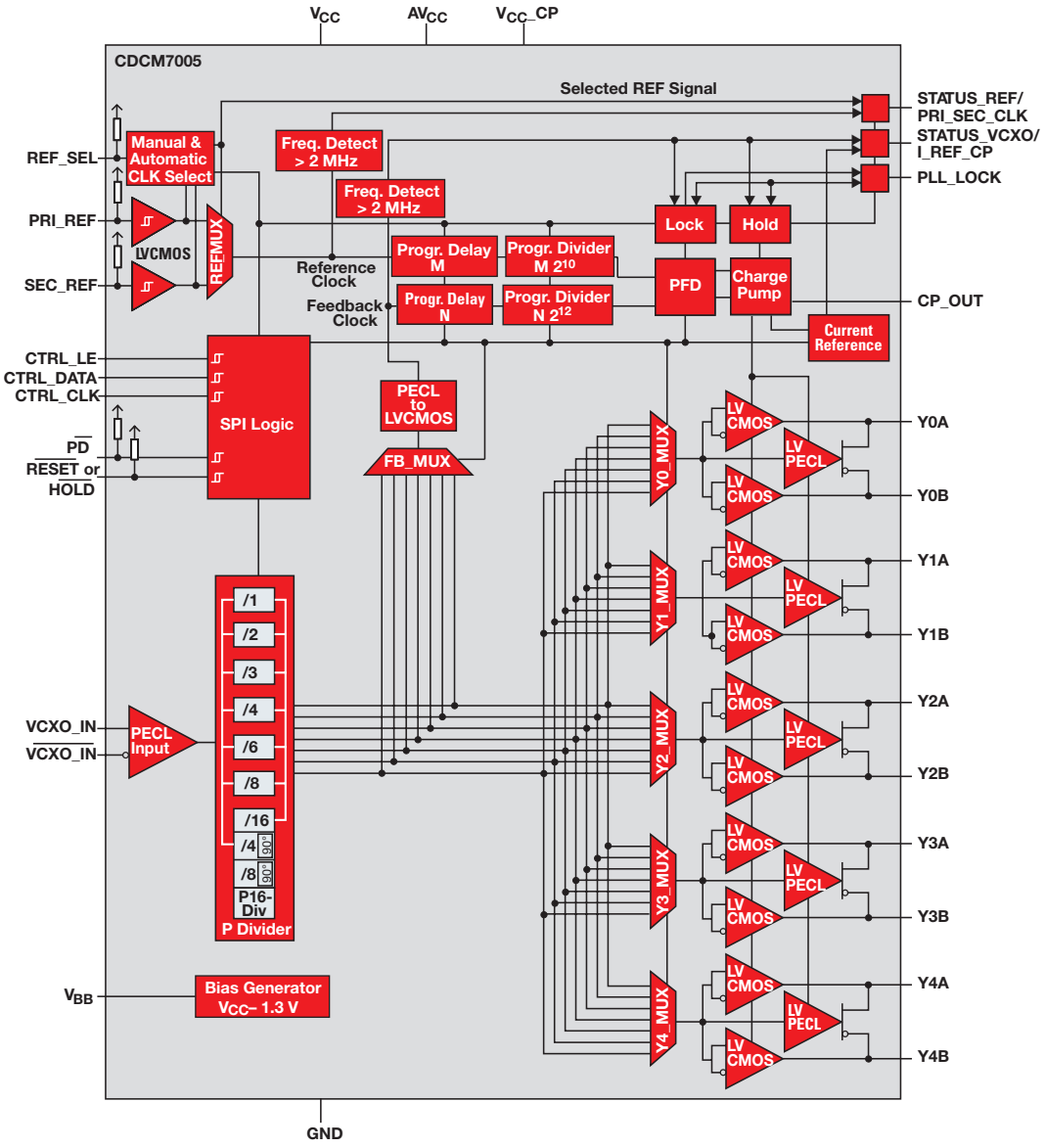
CDCM7005

Get samples, datasheets, and evaluation modules at: **www.ti.com/sc/device/CDCM7005**

The CDCM7005 can lock to one of two reference clock inputs, PRI_REF or SEC_REF. It supports frequency hold-over mode and fast frequency locking for fail-safe and increased system redundancy. The VC(X)O_IN clock operates at up to 2.2 GHz.

Key Features

- High-performance LVPECL and LVCMOS PLL clock synchronizer
- Outputs can be a combination of LVPECL and LVCMOS (up to five differential LVPECL outputs or 10 LVCMOS outputs)
- Output frequency is derived from input frequency divided by 1, 2, 3, 4, 6, 8 or 16 on each individual output
- Analog and digital PLL lock indication
- Provides VBB bias voltage output for single-ended input signals (VCXO_IN)
- SPI-controllable device setting
- Industrial temperature range: –40°C to 85°C
- Packaging: 64-pin BGA (0.8-mm pitch, ZVA) or 48-pin QFN (RGZ)



CDCM7005 functional diagram.

Five Output Clock Generator/Jitter Cleaner with Integrated Dual VCOs

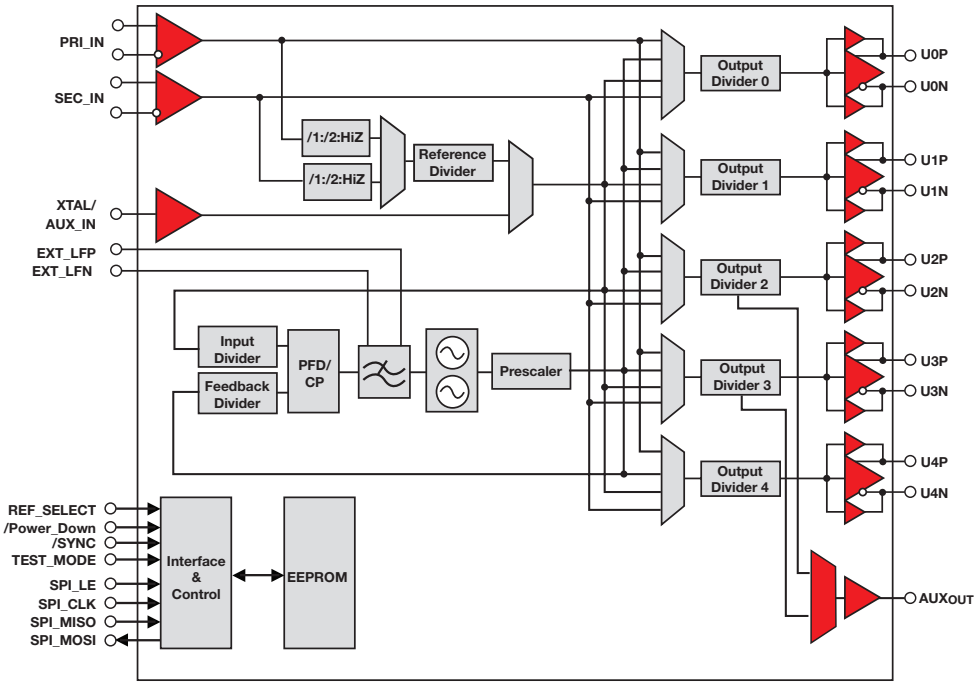
CDCE62005

Get samples, datasheets, evaluation modules and app reports at: **www.ti.com/sc/device/CDCE62005**

The CDCE62005 is a low-jitter clock generator and distributor that features a high degree of configurability via a SPI interface, and programmable start-up modes determined by integrated EEPROM. Specifically tailored for clocking data converters and high-speed digital signals, the CDCE62005 achieves jitter performance well under 1-ps RMS. It incorporates a synthesizer block with partially integrated loop filter, a clock distribution block including programmable output formats, and an input block featuring an innovative smart multiplexer.

Key Features

- Integrated frequency synthesizer including PLL, multiple VCOs and loop filter:
  - Full programmability facilitates phase-noise performance optimization enabling jitter cleaner mode
  - Programmable charge-pump gain and loop filter settings
  - Unique dual-VCO architecture supports a wide tuning range 1.75 GHz to 2.356 GHz
- Universal output blocks support up to 5 differential, 10 single-ended, or combinations of differential or single-ended:
  - 1-ps RMS (10 kHz to 20 MHz) output jitter performance
  - Low output phase noise: (e.g. –130 dBc/Hz at 1-MHz offset, Fc= 491.52 MHz)
  - Output frequency ranges from 4.25 MHz to 1.175 GHz in synthesizer mode
  - Output frequency up to 1.5 GHz in fan-out mode
  - LVPECL, LVDS, LVCMOS and special high-output swing modes
  - Independent output dividers support divide ratios from 1 to 80
  - Independent coarse skew control on all outputs
- Flexible inputs with innovative smart multiplexer feature:
  - Two universal differential inputs accepts frequencies up to 1500 MHz (LVPECL), 800 MHz (LVDS), or 200 MHz (LVCMOS)
  - One auxiliary input accepts single-ended clock source or crystal. Auxiliary input accepts crystals in the range of 2 MHz to 42 MHz or a LVCMOS input up to 150 MHz
  - Clock generator mode using crystal input
  - Smart input multiplexer can be configured to automatically switch between highest priority clock source available allowing for fail-safe operation and holdover modes
- Integrated EEPROM stores default settings; therefore, the device can power up in a known, pre-defined state
- ESD protection exceeds 2-kV HBM
- Industrial Temperature Range –40°C to 85°C
- Packaging: QFN-48



CDCE62005 functional diagram.

Direct Rambus™ Clock Generator (533 MHz with Phase Aligner and 400 MHz without Phase Aligner)

CDCFR83A, CDCR61A

Get samples and datasheets at: **www.ti.com/sc/device/CDCFR83A** or **www.ti.com/sc/device/CDCR61A**

The CDCR61A is an independent clock generator that provides one differential, high-speed, Rambus®-channel-compatible output pair and one single-ended output at half the crystal frequency. The CDCR83A and CDCFR83A provide clock multiplication and phase alignment for Direct Rambus memory systems to enable synchronous communication between the Rambus channel and the ASIC clock domains.

Key Features

CDCFR83A:

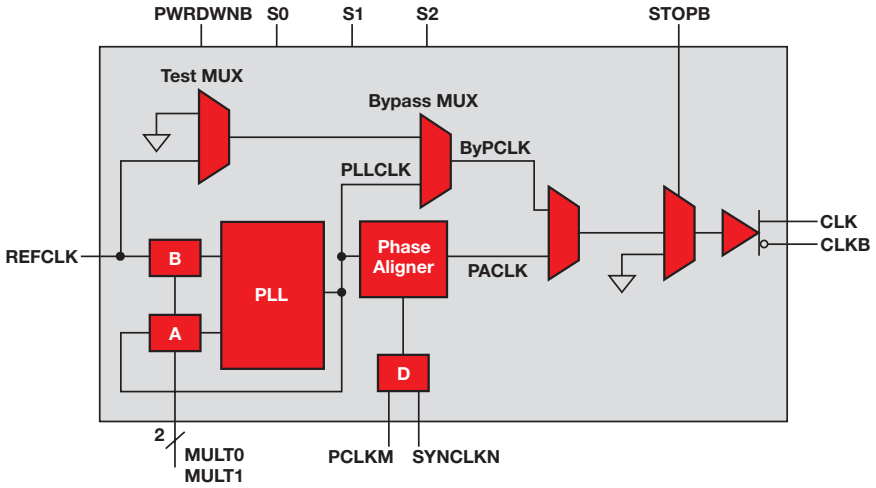
- Wide-input frequency range from 33 to 100 MHz
- Spread-spectrum-clock (SSC) tracking capability to reduce EMI

CDCR61A:

- Requires an external 18.75-MHz crystal oscillator

Applications

- The CDCR61A is a 400-MHz differential clock source for the 800-MHz Direct Rambus clock system
- The CDCR83A and the CDCFR83A provide clock multiplication and phase alignment for Direct Rambus clock system



CDCFR83A/CDCR61A functional diagram.

Rambus® XDR™ Clock Generator

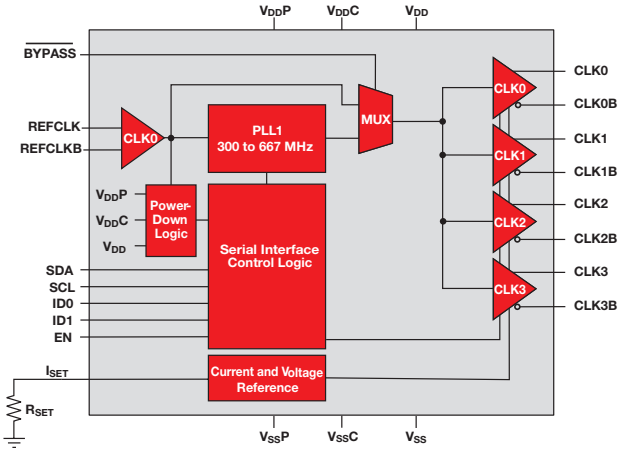
CDCD5704

Get samples and datasheets at: **www.ti.com/sc/device/CDCD5704**

The CDCD5704 clock generator provides the necessary clock signals to support an XDR memory subsystem and Redwood logic interface using a reference clock input with or without spread-spectrum modulation. The CDCD5704 provides an off-the-shelf solution for a broad range of high-performance interface applications.

Key Features

- 300- to 667-MHz clock source for XDR memory subsystems and Redwood logic interface
- Input compatible with spread-spectrum clock (SSC)
- Differential or single-ended reference clock input of 100 or 133 MHz
- Programmable serial interface
- Supports frequency multiplication factors x3, x4, x5, x6, x8, x9/2, x15/2, x15/4
- Low cycle-to-cycle jitter (one to six cycles):
  - 40 ps: 300 to 635 MHz
  - 30 ps: 636 to 667 MHz
- Operates from single 2.5-V supply (±0.125 V)
- Packaging: 28-pin TSSOP



CDCD5704 functional diagram.

28-bit to 56-Bit Registered Buffer with Address-Parity Test

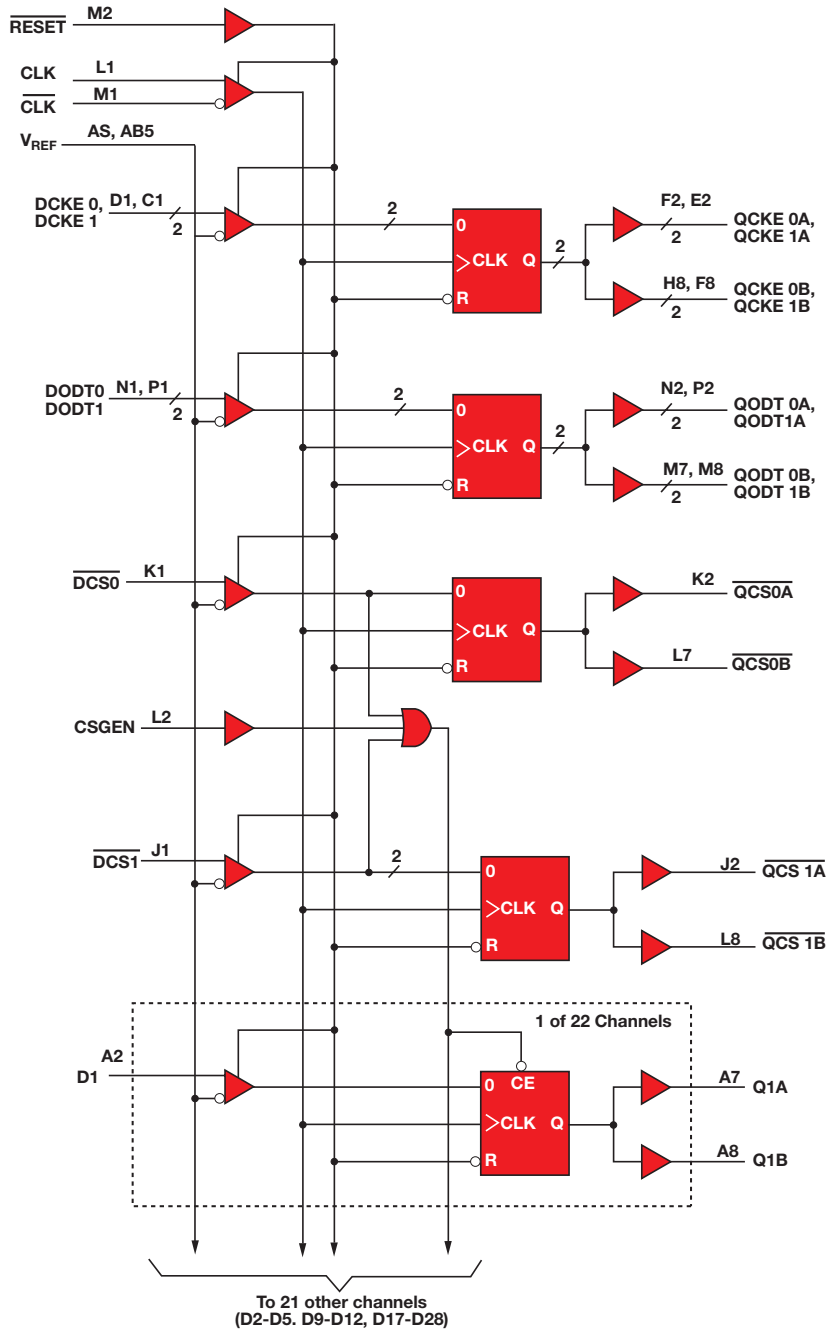
74SSTUB32865, 74SSTUB32865A, 74SSTUB32868, 74SSTUB32868A

Get samples, datasheets and app reports at: **www.ti.com/sc/device/74SSTUB32865, 74SSTUB32865A, 74SSTUB32868, 74SSTUB32868A**

This 28-bit 1:2 configurable registered buffer is designed for 1.7-V to 1.9-V V_{CC} operation. One device per DIMM is required to drive up to 18 SDRAM loads or two devices per DIMM are required to drive up to 36 SDRAM loads. The 74SSTUB32865A and the 74SSTUB32868A include a parity checking function. Parity, which arrives one cycle after the data input to which it applies, is checked on the PAR_IN input of the device. Two clock cycles after the data are registered, the corresponding QERR signal is generated.

Key Features

- Configurable as 28-bit 1:2 registered buffer
- Supports all DDR2 speed nodes, 400, 533, 667 and 800
- Operating frequency up to 410 MHz
- Low-propagation delay from clock input to data output : Max 1.5 nS
- 74SSTUB32865, 74SSTUB32868: 8-mA output current, one device can drive up to 18 SDRAMs
- 74SSTUB32865A, 74SSTUB32868A: 12-mA output current, one device can drive up to 18 stacked SDRAMs
- Supports SSTL_18 data inputs
- Differential clock inputs
- Supports LVCMOS switching levels on the control and RESET inputs
- Checks parity on DIMM independent data input
- Pinout optimizes DDR2 DIMM PCB layout
- Output edge-control circuitry minimizes switching noise
- Industrial temperature range: –40°C to +85°C
- Packaging: 176-ball BGA



Logic diagram for Register-A configuration (positive logic); C=0.

PLL Drivers for DDR2 400/533/667/800

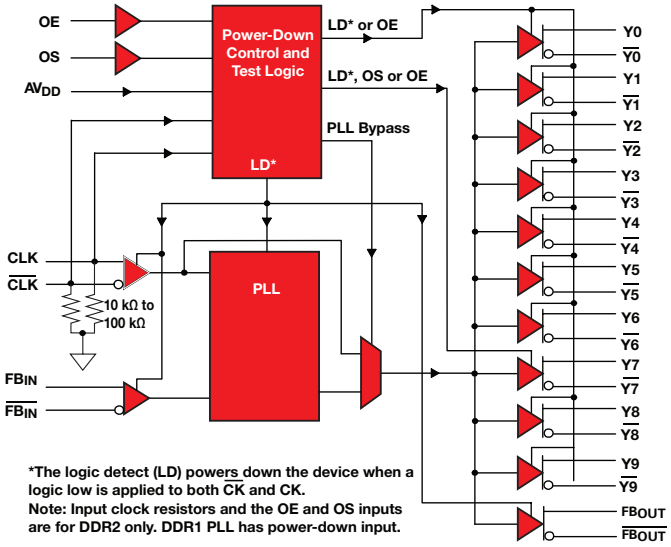
CDCUA877, CDCU2A877

Get samples, datasheets and app reports at: **www.ti.com/sc/device/CDCUA877** or **www.ti.com/sc/device/CDCU2A877**

The CDCUA877 is a high-performance, low-crossover-voltage, low-power, low-skew and low-jitter zero-delay clock buffer that distributes a differential clock input pair to 10 differential pairs of clock outputs and to one differential pair of feedback clock outputs. The CDCU2A877 has a 2x output drive capability. These devices meet or exceed the DDR2 JEDEC specification.

Key Features

- 1.8-/1.9-V PLL for DDR2
- Output current:
  - CDCUA877: 9 mA
  - CDCU2A877: 18 mA
- Operating frequency: 125 to 410 MHz
- Compatible with spread-spectrum clock (SSC)
- Low current consumption: <200 mA typical
- Low cycle-to-cycle jitter: ±40 ps
- Low period jitter: ±30 ps
- Low output skew: 35 ps
- Stabilization time: <6 µs
- Packaging: 52-ball MicroStar Junior™ BGA (0.65-mm pitch)



CDCUA877/CDCUA877 functional diagram.

25-Bit Configurable Registered Buffer with SSTL_18 Inputs and Outputs

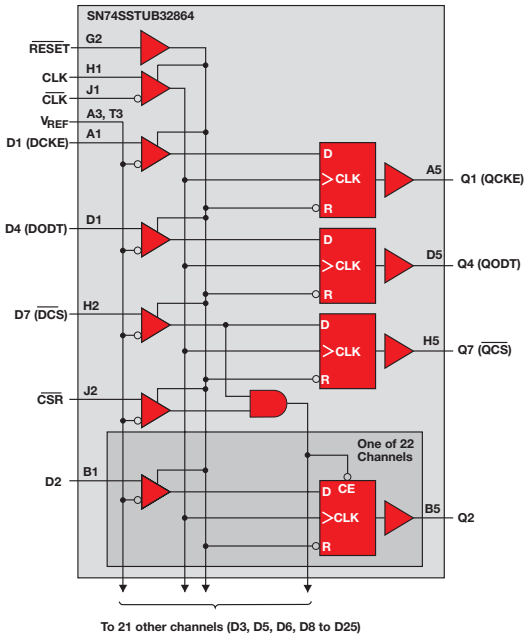
SN74SSTUB32864, SN74SSTUB32866

Get samples, datasheets, and evaluation modules at: **www.ti.com/sc/device/SN74SSTUB32864** or **www.ti.com/sc/device/SN74SSTUB32866**

The SN74SSTUB32864 is configurable as a 1:1 or 1:2 registered buffer, which makes it flexible enough to be used in a multitude of RDIMM configurations. In the 1:1 pinout configuration, only one device per DIMM is required to drive nine SDRAM loads. In the 1:2 pinout configuration, two devices per DIMM are required to drive 18 SDRAM loads. TI also offers the SN74SSTUB32866 for higher-reliability systems. This register has the capability of adding parity to a DDR2 RDIMM. Additional parity I/Os are introduced for the parity calculation. When two devices are used on a DIMM, the register has the capability of cascading the parity path of the two registers while maintaining the same parity output timing as the single-device parity configuration.

Key Features

- Supports DDR2 400/533/667/800
- Pinout optimizes DDR2 DIMM PCB layout
- Configurable as 25-bit 1:1 or 14-bit 1:2 registered buffer
- Chip-select inputs gate the data outputs from changing state and minimize system power consumption
- Output-edge-control circuitry minimizes switching noise in an unterminated line
- Supports SSTL_18 data inputs
- Differential clock inputs
- Checks parity on DIMM-independent data inputs (SN74SSTUB32866)
- Packaging: 96-ball BGA with Junior™ BGA (0.65-mm pitch)



SN74SSTUB32864/SN74SSTUB32866 functional diagram.

28-Bit to 56-Bit Registered Buffer for DDR3

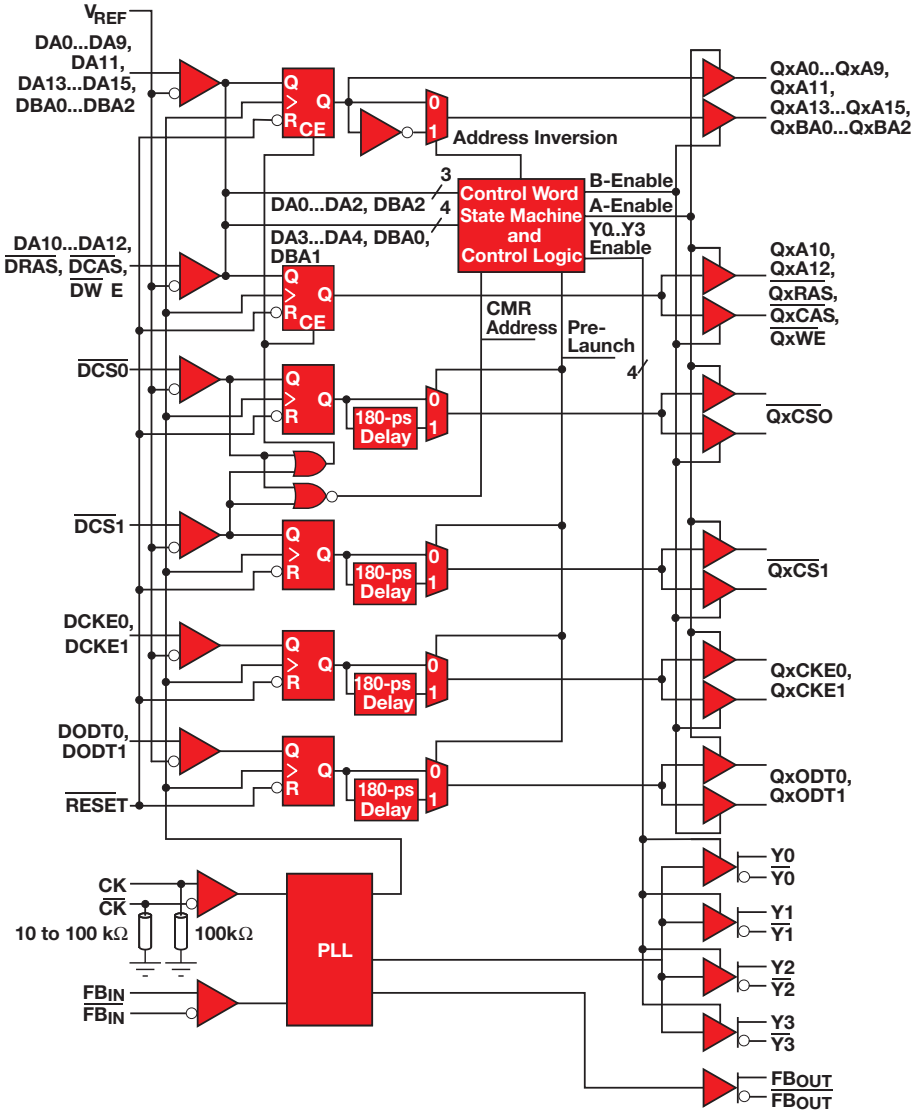
SN74SSQE32882

Get samples, datasheets and app reports at: **www.ti.com/sc/device/SN74SSQE32882**

This JEDEC SSTE32882 compliant 28-bit 1:2 or 26-bit 1:2 and 4-bit 1:1 registering clock driver with parity is designed for operation on DDR3 Registered DIMMs with Vdd of 1.5 V and 1.35 V. Input bus data integrity is protected by a parity function. One register can drive up to 72 SDRAMs on one module. The SN74SSQE32882 implements different power-saving mechanisms to reduce thermal power dissipation and to support system power-down states. Power consumption is further reduced by disabling unused outputs.

Key Features

- PLL integrated register for DDR3 800/1066/1333 at 1.5-V operation voltage
- Operating frequency : 300 to 670 MHz
- V_{CC} = 1.5 V (nominal) and 1.35 V (nominal)
- LVDDR3 800/1067 at 1.35-V operation voltage
- 4Rx4 and 4Rx8
- 1:2 drivers for address/control signals
- Dedicated balls for DIMM-dependent signals : DCS0, DCS1, DCKE0, DCKE1, DODT0, DODT1
- 22-Bits for DIMM-independent signals: address (A0 … A15), RAS, CAS, WE, BA[2:0]
- Drive strength control
- Parity check on DIMM-independent signals
- Support DIMM power-down mode and CKE power-down mode
- One cycle MRS
- Input-to-output jitter cleaning
- Temperature and voltage drift compensation
- External feedback with no external capacitor added
- Low jitter
- Low output skew, tQsk1a
- Low active-mode power consumption
- Temperature range: 0°C to +85°C
- Packaging: 176-ball BGA



SN74SSQE32882 functional diagram.

Integer-N PLL with Integrated VCO

TRF3761 Family

Get samples, datasheets, evaluation modules and app reports at: **www.ti.com/sc/device/TRF3761-A**

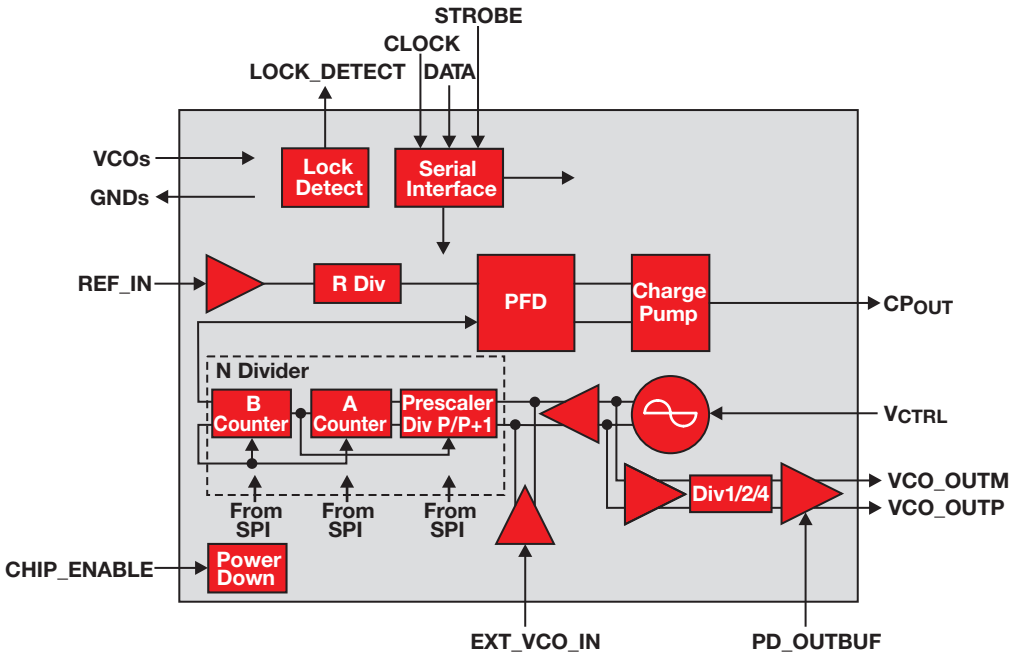
The TRF3761 is a family of high-performance, highly integrated frequency synthesizers optimized for wireless infrastructure applications. The TRF3761 includes a low-noise voltage-controlled oscillator (VCO) and an integer-N PLL. It integrates division options of /2 or /4 for a more flexible output frequency range. It is controlled through a three-wire serial peripheral interface (SPI). It can be powered down when not in use by the SPI or external pin.

Key Features

- Fully integrated VCO
- Low phase noise: –138 dBc/Hz (at 600 kHz, fVCO of 1.9 GHz)
- Low noise floor: –160 dBc/Hz at 10-MHz offset
- Integer-N PLL
- Input reference frequency range: 10 to 104 MHz
- VCO frequency output divided by 1, 2 or 4
- Output buffer enable pin
- Programmable charge-pump current
- Hardware and software power down
- Three-wire serial interface
- Single supply: 4.5-V to 5.25-V operation
- Silicon germanium technology

Applications

- Wireless infrastructure:
  - WCDMA
  - CDMA
  - GSM



TRF3761 functional diagram.

High-Performance Integer-N PLL Frequency Synthesizer

TRF3750

Get samples, datasheets and evaluation modules at: **www.ti.com/sc/device/TRF3750**

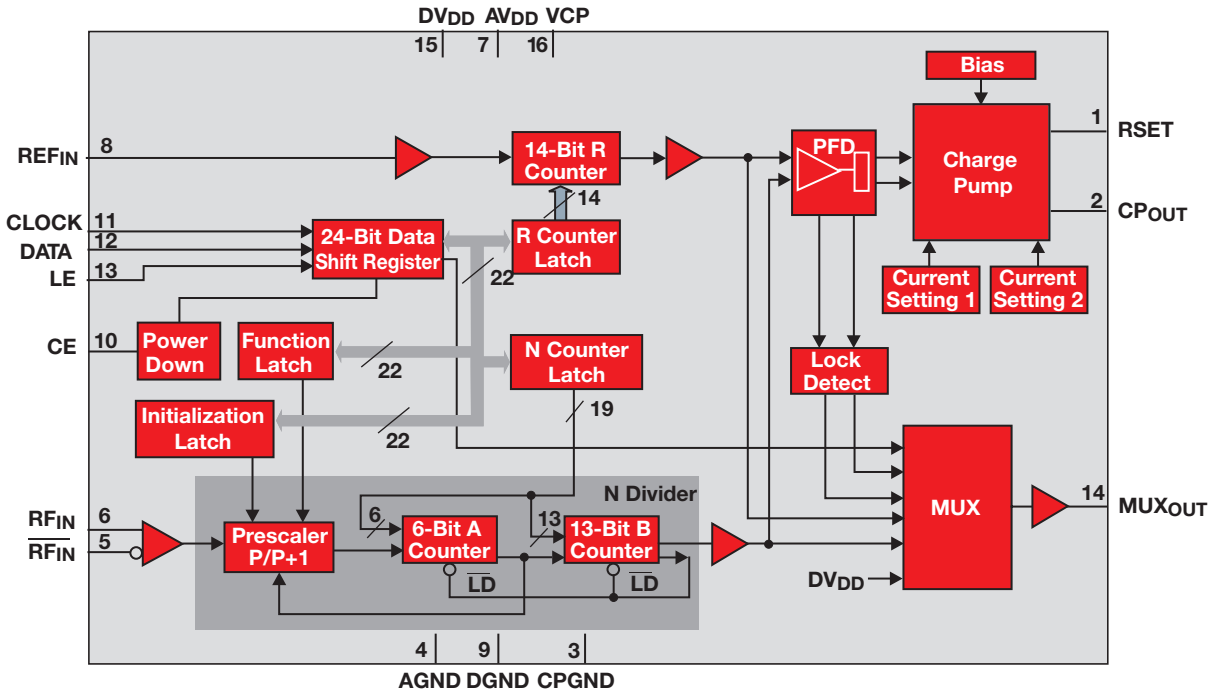
The TRF3750 frequency synthesizer is ideal for designing the local oscillator portion of wireless transceivers by providing complete programmability and ultra-low phase noise. The device features a user-selectable dual-modulus prescaler, a 14-bit reference (R) divider, a 6-bit A counter and a 13-bit B counter. The R divider allows the user to select the desired frequency for the phase-frequency-detector (PFD) circuit and, with the use of the counters, to implement an N divider of value N = A + P x B. With an extended charge-pump supply (VCP) of up to 8 V, a wide variety of external VCOs can be used to complete the phase-locked loop. Ultra-low phase noise and reference spur performance make the TRF3750 ideal for generating the local oscillator in the most demanding wireless applications.

Key Features

- Single device covers frequencies up to 2.4 GHz
- Dual supply range: 3 to 3.6 V and 4.5 to 5.5 V
- Separate VCP up to 8 V
- Simple three-wire serial interface allows for fully programmable:
  - A, B and R counters
  - Dual modulus prescaler (8/9, 16/17, 32/33 and 64/65)
  - Charge-pump current
- Lock-detect output (digital and analog)
- Versatile hardware and software power down
- ESD protection circuitry
- Packaging: 16-pin TSSOP thin quad flatpack and 20-pin 4 x 4-mm QFN

Applications

- Wireless infrastructure:
  - GSM, IS136, EDGE/UWC-136
  - IS95, UMTS, cdma2000®
- Portable wireless communications
- Wireless LAN
- Wireless transceivers
- Communication test equipment



TRF3750 functional diagram for TSSOP package.

M-LVDS Backplane Clock Drivers

M-LVDS Features

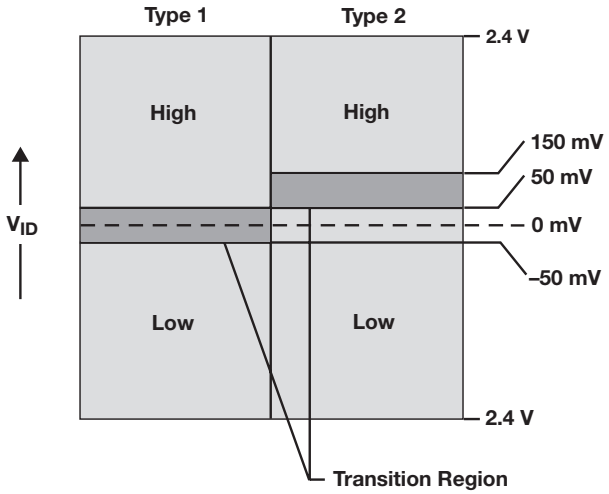
- TIA/EIA-899 standard
- Driver output current
  - 11.3 mA vs. 3.5 mA (LVDS)
- Receiver thresholds
  - 50 mV vs. 100 mV (LVDS)
- Driver edge rate control
  - 1 ns min allows ease-of-stub design
- Contention provisions
  - Driver short circuit limited to 43 mA
  - Drivers, receivers and disabled devices must limit their bus voltage from 0 to 2.4 V
  - Drivers are tested with 32 contending nodes
- Type 2 receivers: internal failsafe (no external bias network)
- –1-V to 3.4-V common mode
- 3.3-V supply operation

M-LVDS for ATCA

- Synchronous ATCA clock signals (8 kHz, 19.22 MHz and user defined <100 MHz) use M-LVDS.

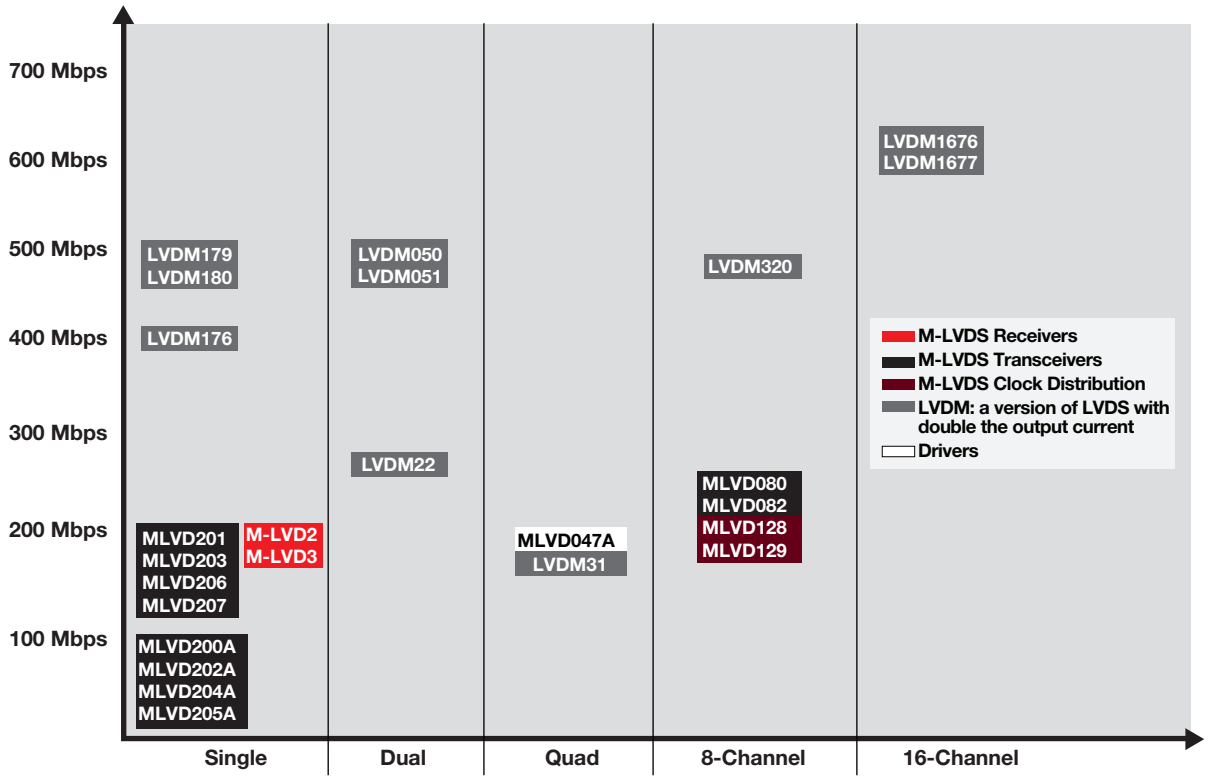
M-LVDS Devices from TI

- TIA/EIA-899 standard compliant guarantees true multipoint
- Type 1 receivers: 25-mV hysteresis to prevent oscillation



Receiver types.

Multipoint LVDS



LVDS Clock Buffers

Design Considerations

Signaling Rate — TI offers repeaters/translators and crosspoint switches with signaling rates up to 4.0 Gbps.

Jitter —Reducing jitter, the deviation of a signal timing event from its ideal position, has become a priority for ensuring reliability in high-speed data buses.

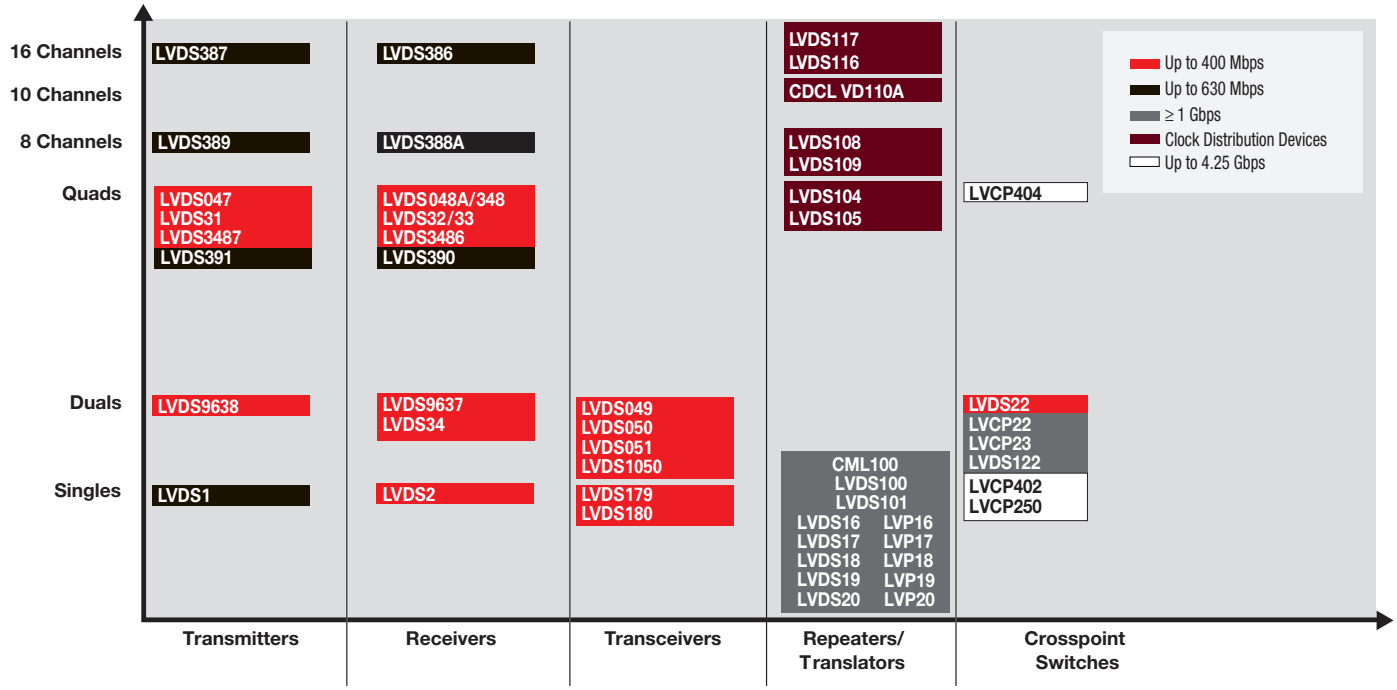
Skew —Excessive skew, the time delta between the actual and expected arrival time of a clock signal, can limit the maximum bandwidth performance and lead to data sampling errors. Low skew specifications make high-speed interconnect devices excellent for signal buffering.

Power Consumption —Low-voltage differential signaling (LVDS) offers a low-power alternative to ECL and PECL devices. Current-mode drivers in LVDS produce a constant current, which allows power consumption to be relatively independent of frequency. The constant current driver delivers about 3.5 mA to a 100-W load.

Technical Information

- LVDS is based on the TIA/EIA-644A standard conceived to provide a general-purpose electrical-layer specification for drivers and receivers connected in a point-to-point or multidrop interface.

LVDS Family of Products



Signaling Rate

There are two bus types available: (1) address/data multiplexed and (2) parallel. With (1), the memory address lines and data lines share the same pins. With (2), the address lines and data lines are separate and the interface is the same as a static RAM. The address/data multiplexed devices have fewer pins but may require more logic to interface.

3- or 5-V Operation

The RTCs can run from a 5-V or 3-V rail.

CPU Supervisor

Some parts include a full CPU supervisor that provides:

- CPU reset (power on and push button)
- Power-fail interrupt
- Watchdog timer
- Non-volatile control for additional NVSRAM

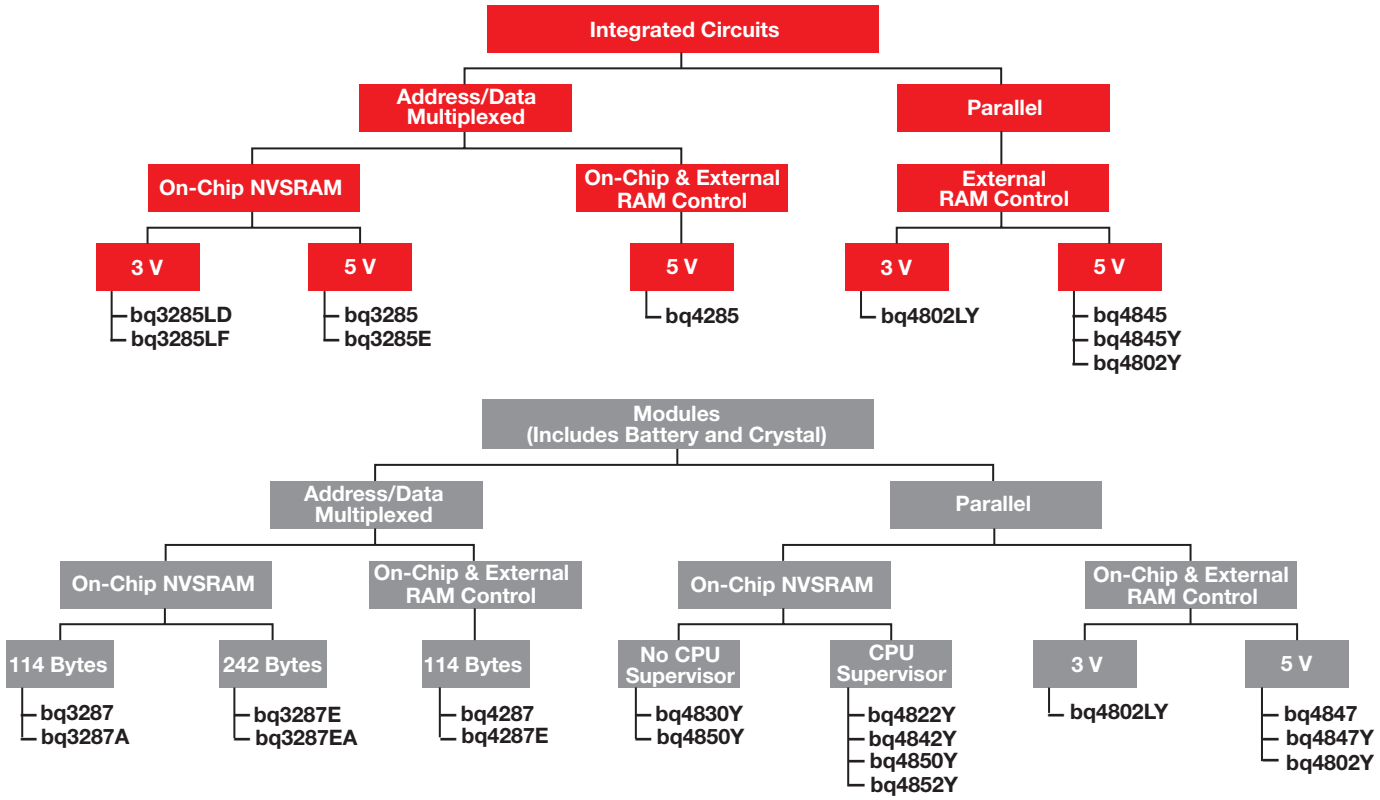
The integration of the supervisor on the RTC can reduce the component count in a design.

- Onboard NVSRAM
- VCC tolerance
- Package type

Features

- Real-time clock counts seconds through centuries in BCD format
- Less than 500 nA of current consumption in battery backup mode
- Clock accuracy (modules) better than 1 minute per month
- Up to 512K x 8 of onboard NVSRAM
- 3- or 5-V operation
- Fully integrated CPU supervisor

Real-Time Clocks (RTCs) Family of Products



For more information, visit
http://clocks.ti.com

Clocks by Function

Non-PLL Clock Buffers

(Device parameters continued on next page.)

Device	Description	Input Level	Output Level	Frequency (MHz)
Differential				
CDCP1803	1:3 buffer with dividers	LVPECL/LVDS	LVPECL	0 to 800
CDCLVP110	1:10 LVPECL/HSTL with selectable input clock	LVPECL/HSTL	LVPECL	0 to 3.5 GHz
CDCLVP111	1:10 LVPECL buffer with input mux	LVPECL	LVPECL	DC to 3.5 GHz
CDCLVP215	Dual1:5 LVPECL buffer	LVPECL	LVPECL	DC to 3.5 GHz
CDCLVD110A	1:10 programmable LVDS clock	LVDS	LVDS	0 to 900
SN65LVEP11	1:2 ECL/PECL buffer	ECL/PECL	ECL/PECL	0 to 3GHz
SN65EL11	1:2 ECL/PECL buffer	ECL/PECL	ECL/PECL	0 to 2.5GHz
CDCL1810	1:10 high-performance clock buffer	LVDS	CML	0 to 650
Single Ended				
CDC203	6:6 inverter/clock driver	CMOS	CMOS	0 to 40
CDC204	6:6 inverter/clock driver	CMOS	CMOS	0 to 80
CDC208	Dual 1:4 fanout, 3-state outputs	TTL	CMOS	0 to 60
CDC318A	1:18 clock with I^2C control interface	LVTTL	LVTTL	0 to 100
CDC319	1:10 clock with I^2C control interface	LVTTL	LVTTL	0 to 140
CDC328A	1:6 fanout with selectable polarity	TTL	TTL	0 to 100
CDC329A	1:6 fanout with selectable polarity	TTL	CMOS	0 to 80
CDC337	1:8 clock with four 1x outputs, four 1/2x outputs, 3-state outputs	TTL	CMOS	0 to 80
CDC339	1:8 clock with four 1x outputs, four 1/2x outputs, 3-state outputs	TTL	CMOS	0 to 80
CDC340	1:8 with fast tpd fanout	TTL	TTL/CMOS	0 to 80
CDC341	1:8 with fast tpd fanout	TTL	TTL/CMOS	0 to 80
CDC351	1:10 with fast tpd fanout, 3-state outputs	LVTTL	LVTTL/LVCMOS	0 to 100
CDC351I	1:10 with fast tpd fanout, 3-state outputs	LVTTL	LVTTL/LVCMOS	0 to 100
CDC391	1:6 clock with selectable polarity and 3-state outputs	TTL	TTL	0 to 100
CDCV304	1:4 fanout for PCI-X and general apps	LVTTL	LVCMOS	0 to 200
CDCVF310	1:10 clock with 2 banks for general-purpose apps	LVTTL	LVTTL	0 to 200
CDCVF2310	1:10 clock with 2 banks for general-purpose apps, series output resistors	LVTTL/LVCMOS	LVTTL/LVCMOS	0 to 170 (VDD = 2.5 V), 0 to 200 (VDD = 3.3 V)
CDC2351	1:10 with fast tpd fanout, 3-state outputs, series output resistors	LVTTL	LVTTL/LVCMOS	0 to 100
Mixed: Differential and Single Ended				
CDCM1804	1:3 LVPECL + 1 LVCMOS with dividers	LVPECL	LVPECL/LVCMOS	800
CDCM1802	1:1 LVCMOS + 1 LVPECL with dividers	LVPECL	LVPECL/LVCMOS	800
CDCE18005	1:5 LVPECL/LVDS/LVCMOS buffer with dividers	LVPECL/LVDS/LVCMOS	LVPECL/LVDS/LVCMOS	DC to 1.5 GHz

PLL Clock Buffers

Device	Description	Input Level	Output Level	Frequency (MHz)
Zero-Delay PLL: Differential				
CDCV850	1:10 differential clock driver	SSTL_2/universal	SSTL_2	60 to 140
CDCV855	1:4 differential clock driver	SSTL_2/ LVTTL	SSTL_2	60 to 180
CDCV857	1:10 PLL differential clock driver for DDR 200/266/333, SSC	SSTL_2/ LVTTL	SSTL_2	60 to 200
CDCV857A	1:10 PLL differential clock driver for DDR 200/266/333, SSC	SSTL_2/ LVTTL	SSTL_2	60 to 180
CDCV857B	1:10 PLL differential clock driver for DDR 200/266/333, SSC	SSTL_2/ LVTTL	SSTL_2	60 to 200
CDCV857BI	1:10 PLL differential clock driver for DDR 200/266/333, SSC	SSTL_2/ LVTTL	SSTL_2	60 to 200
CDCVF857	1:10 PLL differential clock driver for DDR 200/266/333/400, SSC	SSTL_2/ LVTTL	SSTL_2	60 to 220

New products are listed in bold red.

(Device parameters continued from previous page.)

Device	V_{CC} (V)	Propagation Delay	Output Skew (max) (ps)	Char. Temp. (°C)	Package(s)	Price*
Differential						
CDCP1803	3.3	320 to 600 ps	30 ps	–40 to 85	24/QFN	3.15
CDCLVP110	2.5/3.3	230 to 370 ps	30 ps	–40 to 85	32/LQFP	5.55
CDCLVP111	2.5/3.3V	230 to 370 ps	30 ps	–40 to 85	32LQFP/32QFN	6.10
CDCLVP215	2.5/3.3V	230 to 370 ps	30 ps	–40 to 85	32/LQFP	6.10
CDCLVD110A	2.5	3 ns	30 ps (typ)	–40 to 85	32/TQFP	5.90
SN65LVEP11	2.5/3.3	200 to 300 ps	15 ps	–40 to 85	8/SOIC, 8/MSOP	5.50
SN65EL11	5	200 to 300 ps	15 ps	–40 to 85	8/SOIC, 8/MSOP	2.40
CDCL1810	1.8	3 ns	64 ps	–40 to 85	48/QFN	6.00
Single Ended						
CDC203	3.3	3.5 to 6.1 ns	0.7 ns	–25 to 70	20/SOIC	3.45
CDC204	5	2.9 to 5.7 ns	1 ns	25 to 70	20/SOIC	3.00
CDC208	5	3.6 to 11.7 ns	1 ns	–40 to 85	20/SOIC	4.10
CDC318A	3.3	1.2 to 4.5 ns	250 ps	0 to 70	48/SSOP	1.45
CDC319	3.3	1.2 to 3.6 ns	250 ps	0 to 70	28/SSOP	1.50
CDC328A	5	1.5 to 5.0 ns	500 ps	–40 to 85	16/SOIC/SSOP	3.55
CDC329A	5	1.7 to 5.9 ns	600 ps	–40 to 85	16/SOIC	3.10
CDC337	5	4 to 9 ns	900 ps	–40 to 85	20/SOIC	4.20
CDC339	5	3 to 9 ns	900 ps	–40 to 85	20/SOIC/SSOP	3.50
CDC340	5	2.8 to 4.8 ns	600 ps	0 to 70	20/SOIC	4.20
CDC341	5	3.1 to 4.9 ns	600 ps	0 to 70	20/SOIC	4.50
CDC351	3.3	3 to 4.2 ns	500 ps	0 to 70	24/SOIC/SSOP	5.65
CDC351I	3.3	—	600 ps	–40 to 85	24/SOIC/SSOP	5.65
CDC391	5	1.5 to 5.0 ns	500 ps	–40 to 85	16/SOIC	3.40
CDCV304	2.5/3.3	1.8 to 3.0 ns	100 ps	–40 to 85	8/TSSOP	1.10
CDCVF310	2.5/3.3	1.0 to 2.8 ns (VDD = 3.3 V), 1.3 to 4.0 ns (VDD = 2.5 V)	150 ps @ 3.3 V, 230 ps @ 2.5 V	–40 to 85	24/TSSOP	2.05
CDCVF2310	2.5/3.3	1.3 to 2.8 ns (VDD = 3.3 V), 1.5 to 3.5 ns (VDD = 2.5 V)	100 ps @ 3.3 V, 170 ps @ 2.5 V	–40 to 85	24/TSSOP	2.05
CDC2351	3.3	3.6 to 4.8 ns	500 ps	0 to 70	24/SOIC/SSOP	5.20
Mixed: Differential and Single Ended						
CDCM1804	3.3	600 ps (LVPECL), 2.6 ns (LVCMOS)	30 ps (LVPECL), 1.6 ns (LVCMOS)	–40 to 85	24/QFN	5.50
CDCM1802	3.3	600 ps (LVPECL), 2.6 ns (LVCMOS)	1.6 ns (typ)	–40 to 85	16/QFN	3.75
CDCE18005	3.3	4 ns	75 ps	-40 to 85	48/QFN	5.96

Device	V_{CC} (V)	Jitter (Peak-to-Peak [P-P] or Cycle-to-Cycle [C-C])	Phase Error	Output Skew (max) (ps)	Char. Temp. (°C)	Package(s)	Price*
Zero-Delay PLL: Differential							
CDCV850	2.5	C-C: ±30 ps (100 to 133 MHz)	–80/150 ps (133 MHz)	75	–40 to 85	48/TSSOP	1.65
CDCV855	2.5	C-C: ±50 ps (100 to 180 MHz)	±100 ps (100 to 180 MHz)	50	–40 to 85	28/TSSOP	1.60
CDCV857	2.5	C-C: ±75 ps (100 to 200 MHz)	–150/50 ps (200 MHz)	75	0 to 85	48/TSSOP	3.90
CDCV857A	2.5	C-C: ±50 ps (100 to 180 MHz)	±100 ps (100 to 180 MHz)	75	0 to 85	48/TSSOP, 56/µBGA[1]	2.65
CDCV857B	2.5	C-C: ±50 ps (100 to 200 MHz)	±50 ps (min/max) (100 to 200 MHz)	70 (typ)	0 to 70	48/TSSOP, 56/µBGA[1]	3.35
CDCV857BI	2.5	C-C: ±50 ps (100 to 200 MHz)	±50 ps (min/max) (100 to 200 MHz)	70 (typ)	–40 to 85	48/TSSOP, 56/µBGA[1]	3.35
CDCVF857	2.5	C-C: ±35 ps (133 to 200 MHz)	±50 ps (min/max) (100 to 200 MHz)	40	–40 to 85	48/TSSOP, 48/QFN, 56/µBGA[1]	3.35

[1] *MicroStar BGA™.* **Suggested resale price in U.S. dollars in quantities of 1,000.*

New products are listed in bold red.

Clocks by Function

PLL Clock Buffers (Continued)

(Device parameters continued on next page.)

Device	Description	Input Level	Output Level	Frequency (MHz)
Zero-Delay PLL: Differential				
CDCU877	1:10 PLL differential clock driver for DDR2 applications, SSC	SSTL_18	SSTL_18	10 to 400
CDCU877A	1:10 PLL differential clock driver for DDR2 applications, SSC	SSTL_18	SSTL_18	10 to 400
CDCU877B	1:10 PLL differential clock driver for DDR2 400/533, SSC	SSTL_18	SSTL_18	10 to 340
CDCUA877	1:10 PLL differential clock driver for DDR2 400~800, SSC, 8-mA output	SSTL_18	SSTL_18	125 to 410
CDCU2A877	1:10 PLL differential clock driver for DDR2 400~800, SSC, 16-mA output	SSTL_18	SSTL_18	125 to 410

General Purpose Clock Generator/Synthesizer

Device	Description	Input Level	Output Level	Frequency (MHz)
Programmable/SSC: Non VCXO				
CDCE706	3.3-V programmable 3-PLL clock generator with EEPROM	Crystal/single-ended/differential	2.5- to 3.3-V LVTTL	<300
CDCE906	3.3-V programmable 3-PLL clock generator with EEPROM	Crystal/single-ended/differential	2.5- to 3.3-V LVTTL	<167
CDC706	3.3-V programmable 3-PLL clock generator	Crystal/single-ended/differential	2.5- to 3.3-V LVTTL	<300
CDC906	3.3-V programmable 3-PLL clock generator	Crystal/single-ended/differential	2.5- to 3.3-V LVTTL	<167
CDCDLP223	Clock synthesizer for DLP®	Crystal	LVTTL/HCLK	20 to 400
Programmable/SSC: VCXO				
CDCE913	1.8-V programmable 1-PLL VCXO clock synthesizer with 3.3-V outputs	Crystal/VCXO/single-ended	3.3-V LVTTL	<230
CDCEL913	1.8-V programmable 1-PLL VCXO clock synthesizer with 1.8-V outputs	Crystal/VCXO/single-ended	1.8-V LVTTL	<230
CDCE925	1.8-V programmable 2-PLL VCXO clock synthesizer with 3.3-V outputs	Crystal/VCXO/single-ended	3.3-V LVTTL	<230
CDCEL925	1.8-V programmable 2-PLL VCXO clock synthesizer with 1.8-V outputs	Crystal/VCXO/single-ended	1.8-V LVTTL	<230
CDCE937	1.8-V programmable 3-PLL VCXO clock synthesizer with 3.3-V outputs	Crystal/VCXO/single-ended	3.3-V LVTTL	<230
CDCEL937	1.8-V programmable 3-PLL VCXO clock synthesizer with 1.8-V outputs	Crystal/VCXO/single-ended	1.8-V LVTTL	<230
CDCE949	1.8-V programmable 4-PLL VCXO clock synthesizer with 3.3-V outputs	Crystal/VCXO/single-ended	3.3-V LVTTL	<230
CDCEL949	1.8-V programmable 4-PLL VCXO clock synthesizer with 1.8-V outputs	Crystal/VCXO/single-ended	1.8-V LVTTL	<230
Motherboard				
CDC950	Differential clock synthesizer/driver for PC motherboards	Crystal or other	HSCL	33, 48, 100, 133
CDC960	200-MHz clock synthesizer/driver with spread-spectrum and device-control interface	Crystal or other	LVTTL, HCLK	33, 48, 100, 133
Rambus®				
CDCR61A	400-MHz Direct Rambus™ clock generator-lite, SSC	CMOS	RSL6 (Rambus signaling)	300 to 400
CDCR83A	400-MHz Direct Rambus clock generator, SSC	CMOS	RSL6 (Rambus signaling)	267 to 400
CDCFR83A	533-MHz Direct Rambus clock generator, SSC	CMOS	RSL6 (Rambus signaling)	267 to 533
CDCD5704	XDR™ clock generator	HCLK	XDR RSL	300 to 667
SSC Generator				
CDCS502	1:1 spread spectrum clock multiplier	Crystal	3.3-V LVTTL/ LVCMOS	8 to 108
CDCS503	1:1 spread spectrum clock multiplier	LVCMOS	3.3-V LVTTL/ LVCMOS	DC to 110

New products are listed in bold red.

(Device parameters continued from previous page.)

Device	V_{CC} (V)	Jitter (Peak-to-Peak [P-P] or Cycle-to-Cycle [C-C])	Phase Error	Output Skew (max) (ps)	Char. Temp. (°C)	Package(s)	Price*
Zero-Delay PLL: Differential							
CDCU877	1.8	C-C: ±30 ps (190 to 340 MHz)	±50 ps	35	–40 to 85	52/56/µBGA[1], 40/QFN	2.80
CDCU877A	1.8	C-C: ±30 ps (190 to 340 MHz)	±50 ps	35	–40 to 85	52/56/µBGA[1], 40/QFN	2.80
CDCU877B	1.8	C-C: ±30 ps (190 to 340 MHz)	±50 ps	25	–40 to 85	52/µBGA[1]	2.80
CDCUA877	1.8	C-C: ±40 ps (200 to 333 MHz)	±50 ps	35	–40 to 85	52/µBGA[1]	3.10
CDCU2A877	1.8	C-C: ±40 ps (160 to 410 MHz)	±50 ps	35	0 to 70	52/µBGA[1]	3.10

Device	V_{CC} (V)	Jitter (Peak-to-Peak [P-P]or Cycle-to-Cycle [C-C])	Phase Error	Char. Temp. (°C)	Output Skew (max) (ps)	Package(s)	Price*
Programmable/SSC: Non VCXO							
CDCE706	3.3	60 ps (typ)	—	200	–40 to 85	20/TSSOP	3.60
CDCE906	3.3	60 ps (typ)	—	200	0 to 70	20/TSSOP	2.20
CDC706	3.3	60 ps (typ)	—	200	–40 to 85	20/TSSOP	3.60
CDC906	3.3	60 ps (typ)	—	200	0 to 70	20/TSSOP	2.20
CDCDLP223	3.3	Period jitter: ±75 ps	—	—	–40 to 85	20/TSSOP	2.90
Programmable/SSC: VCXO							
CDCE913	1.8/3.3	60 ps (typ)	—	150	–40 to 85	14/TSSOP	1.60
CDCEL913	1.8/3.3	60 ps (typ)	—	150	–40 to 85	14/TSSOP	1.60
CDCE925	1.8/3.3	60 ps (typ)	—	150	–40 to 85	16/TSSOP	1.80
CDCEL925	1.8/3.3	60 ps (typ)	—	150	–40 to 85	16/TSSOP	1.80
CDCE937	1.8/3.3	60 ps (typ)	—	150	–40 to 85	20/TSSOP	2.15
CDCEL937	1.8/3.3	60 ps (typ)	—	150	–40 to 85	20/TSSOP	2.15
CDCE949	1.8/3.3	60 ps (typ)	—	150	–40 to 85	24/TSSOP	2.35
CDCEL949	1.8/3.3	60 ps (typ)	—	150	–40 to 85	24/TSSOP	2.35
Motherboard							
CDC950	3.3	—	—	—	0 to 85	48/TSSOP	1.30
CDC960	3.3	—	—	—	0 to 70	48/SSOP	1.75
Rambus®							
CDCR61A	1.8/3.3	C-C: 100 ps (400 MHz)	—	—	0 to 85	16/TSSOP	1.60
CDCR83A	3.3	C-C: 50 ps (400 MHz)	±100 ps	—	–40 to 85	24/SSOP	1.75
CDCFR83A	3.3	C-C: 40 ps (533 MHz)	±100 ps	—	–40 to 85	24/SSOP	2.00
CDCD5704	2.5	C-C: 40 ps (300 to 635 MHz)	—	—	0 to 70	28/TSSOP	2.95
SSC Generator							
CDCS502	3.3	60 ps (typ)	—	—	–40 to 85	8/TSSOP	0.95
CDCS503	3.3	60 ps (typ)	—	—	–40 to 85	8/TSSOP	0.95

[1] *MicroStar BGA™.* **Suggested resale price in U.S. dollars in quantities of 1,000.*

New products are listed in bold red.

Clocks by Function

<1-ps RMS Jitter Generator/Synthesizers/Jitter Cleaners

(Device parameters continued on next page.)

Device	Description	Input Level	Output Level	Frequency (MHz)
Integrated VCO				
CDC421125	Low-jitter clock generator for 125-MHz ethernet	Crystal/single-ended	LVPECL	125
CDC421156	Low-jitter clock generator for 156.25-MHz 10G ethernet	Crystal/single-ended	LVPECL	156.25
CDC421312	Low-jitter clock generator for 312.50-MHz 10G ethernet	Crystal/single-ended	LVPECL	312.5
CDC421106	Low-jitter clock generator for 106.25-MHz fibre channel	Crystal/single-ended	LVPECL	106.25
CDC421212	Low-jitter clock generator for 212.25-MHz fibre channel	Crystal/single-ended	LVPECL	212.5
CDC421100	Low-jitter clock generator for 100-MHz PCI Express	Crystal/single-ended	LVPECL	100
CDC421250	Low-jitter clock generator for 250-MHz PCI Express	Crystal/single-ended	LVPECL	250
CDCE421	Flexible low-jitter clock generator, 10 MHz to 1.1 GHz	Crystal/single-ended	LVPECL	11 to 1100
CDCE62005	3:5 generator	Crystal/differential/single-ended	LVPECL/LVDS/LVCMOS	4.25 to 1175
CDCM61001	1:1 generator	Crystal/differential/single-ended	LVPECL/LVDS/LVCMOS	62.5, 74.25, 75, 100, 106.25, 125, 150, 155.52, 156.25, 212.5, 250, 311.04, 312.5, 622.08, 625; LVCMOS output frequency up to 250 MHz
CDCM61002	1:2 generator	Crystal/differential/single-ended	LVPECL/LVDS/LVCMOS	62.5, 74.5, 75, 100, 106.25, 125, 150, 155.52, 156.25, 212.5, 250, 311.04, 312.5, 622.08, 625; LVCMOS output frequency up to 250 MHz
CDCM61004	1:4 generator	Crystal/differential/single-ended	LVPECL/LVDS/LVCMOS	62.5, 74.5, 75, 100, 106.25, 125, 150, 155.52, 156.25, 212.5, 250, 311.04, 312.5, 622.08, 625; LVCMOS output frequency up to 250 MHz
External VCXO				
CDCM7005	Clock synchronizer and jitter cleaner	LVCMOS/LVPECL	LVCMOS/LVPECL	0 to 1500
CDCE72010	2:10 synchronizer	Differential/single-ended	LVPECL/LVDS/LVCMOS	1250

Oscillator ICs

Device	Description	Input Level	Output Level	Frequency (MHz)
PLL				
CDCE421	Flexible low-jitter clock generator, 10 MHz to 1.1 GHz	Crystal/single-ended	LVPECL	11 to 1100
CDCE62005	3:5 generator	Crystal/differential/single-ended	LVPECL/LVDS/ LVCMOS	4.25 to 1175
CDCM61001	1:1 generator	Crystal/differential/single-ended	LVPECL/LVDS/ LVCMOS	62.5, 74.25, 75, 100, 106.25, 125, 150, 155.52, 156.25, 212.5, 250, 311.04, 312.5, 622.08, 625; LVCMOS output frequency up to 250 MHz
CDCM61002	1:2 generator	Crystal/differential/single-ended	LVPECL/LVDS/ LVCMOS	62.5, 74.5, 75, 100, 106.25, 125, 150, 155.52, 156.25, 212.5, 250, 311.04, 312.5, 622.08, 625; LVCMOS output frequency up to 250 MHz
CDCM61004	1:4 generator	Crystal/differential/single-ended	LVPECL/LVDS/ LVCMOS	62.5, 74.5, 75, 100, 106.25, 125, 150, 155.52, 156.25, 212.5, 250, 311.04, 312.5, 622.08, 625; LVCMOS output frequency up to 250 MHz
CDCE913	1.8-V programmable 1-PLL VCXO clock synthesizer with 3.3-V outputs	Crystal/VCXO/single-ended	3.3-V LVTTL	<230
CDCEL913	1.8-V programmable 1-PLL VCXO clock synthesizer with 1.8-V outputs	Crystal/VCXO/single-ended	1.8-V LVTTL	<230
CDCE925	1.8-V programmable 2-PLL VCXO clock synthesizer with 3.3-V outputs	Crystal/VCXO/single-ended	3.3-V LVTTL	<230
CDCEL925	1.8-V programmable 2-PLL VCXO clock synthesizer with 1.8-V outputs	Crystal/VCXO/single-ended	1.8-V LVTTL	<230
CDCE937	1.8-V programmable 3-PLL VCXO clock synthesizer with 3.3-V outputs	Crystal/VCXO/single-ended	3.3-V LVTTL	<230
CDCEL937	1.8-V programmable 3-PLL VCXO clock synthesizer with 1.8-V outputs	Crystal/VCXO/single-ended	1.8-V LVTTL	<230
CDCE949	1.8-V programmable 4-PLL VCXO clock synthesizer with 3.3-V outputs	Crystal/VCXO/single-ended	3.3-V LVTTL	<230
CDCEL949	1.8-V programmable 4-PLL VCXO clock synthesizer with 1.8-V outputs	Crystal/VCXO/single-ended	1.8-V LVTTL	<230
CDCS502	1:1 spread spectrum clock multiplier	Crystal	3.3-V LVTTL/ LVCMOS	8 to 108
Non-PLL				
CDCE401	Oscillator IC with electronic calibration	Crystal	LVCMOS	625 kHz to 100 MHz

New products are listed in bold red. Preview products are listed in bold blue.

(Device parameters continued from previous page.)

Device	V_{CC} (V)	Jitter (Peak-to-Peak [P-P]or Cycle-to-Cycle [C-C])	Phase Error	Output Skew (max) (ps)	Char. Temp. (°C)	Packages(s)	Price*
Integrated VCO							
CDC421125	3.3	—	<1 ps rms	—	–40 to 85	24/QFN	7.70
CDC421156	3.3	—	<1 ps rms	—	–40 to 85	24/QFN	7.70
CDC421312	3.3	—	<1 ps rms	—	–40 to 85	24/QFN	7.70
CDC421106	3.3	—	<1 ps rms	—	–40 to 85	24/QFN	7.70
CDC421212	3.3	—	<1 ps rms	—	–40 to 85	24/QFN	7.70
CDC421100	3.3	—	<1 ps rms	—	–40 to 85	24/QFN	7.70
CDC421250	3.3	—	<1 ps rms	—	–40 to 85	24/QFN	7.70
CDCE421	3.3	—	<1 ps rms	—	–40 to 85	24/QFN	7.70
CDCE62005	3.3	—	<1 ps rms	TBD	–40 to 85	48/QFN	8.25
CDCM61001	3.3	—	<1 ps rms	TBD	–40 to 85	20/QFN	4.55
CDCM61002	3.3	—	<1 ps rms	TBD	–40 to 85	28/QFN	5.50
CDCM61004	3.3	—	<1 ps rms	TBD	–40 to 85	32/QFN	7.15
External VCXO							
CDCM7005	3.3	<1 ps rms	–200/+100 ps	50	–40 to 85	64/BGA, 48/QFN	10.75
CDCE72010	3.3	—	<1 ps rms	50	–40 to 85	64/QFN	12.05

Device	V_{CC} (V)	Jitter (Peak-to-Peak [P-P]or Cycle-to-Cycle [C-C])	Phase Error	Output Skew (max) (ps)	Char. Temp. (°C)	Package(s)	Price*
PLL							
CDCE421	3.3	—	<1 ps rms	—	–40 to 85	Die, 24/QFN	TBD
CDCE62005	3.3	—	<1 ps rms	TBD	–40 to 85	48/QFN	8.25
CDCM61001	3.3	—	<1 ps rms	TBD	–40 to 85	20/QFN	4.55
CDCM61002	3.3	—	<1 ps rms	TBD	–40 to 85	28/QFN	5.50
CDCM61004	3.3	—	<1 ps rms	TBD	–40 to 85	32/QFN	7.15
CDCE913	1.8/3.3	60 ps (typ)	—	150	–40 to 85	14/TSSOP	1.60
CDCEL913	1.8/3.3	60 ps (typ)	—	150	–40 to 85	14/TSSOP	1.60
CDCE925	1.8/3.3	60 ps (typ)	—	150	–40 to 85	16/TSSOP	1.80
CDCEL925	1.8/3.3	60 ps (typ)	—	150	–40 to 85	16/TSSOP	1.80
CDCE937	1.8/3.3	60 ps (typ)	—	150	–40 to 85	20/TSSOP	2.15
CDCEL937	1.8/3.3	60 ps (typ)	—	150	–40 to 85	20/TSSOP	2.15
CDCE949	1.8/3.3	60 ps (typ)	—	150	–40 to 85	24/TSSOP	2.35
CDCEL949	1.8/3.3	60 ps (typ)	—	150	–40 to 85	24/TSSOP	2.35
CDCS502	3.3	60ps (typ)	—	—	–40 to 85	8/TSSOP	0.95
Non-PLL							
CDCE401	2.3 to 3.3	—	—	—	–40 to 85	Die, 8/QFN	TBD

Suggested resale in U.S. dollars in quantities of 1,000)

New products are listed in bold red. Preview products are listed in bold blue.

Clocks by Application

Memory Interface

(Device parameters continued on next page.)

Device	Description	Input Level	Output Level	Frequency (MHz)
SDR				
CDCVF2509A	1:9 low-power PLL clock for PC133 and beyond apps, SSC	LVTTL	LVTTL	50 to 175
CDCVF2510A	1:10 low-power PLL clock driver for PC133 and beyond apps, SSC	LVTTL	LVTTL	50 to 175
DDR PLL				
CDCV850	1:10 differential clock driver	SSTL_2/Universal	SSTL_2	60 to 140
CDCV855	1:4 differential clock driver	SSTL_2/ LVTTL	SSTL_2	60 to 180
CDCV857	1:10 PLL differential clock driver for DDR 200/266/333, SSC	SSTL_2/ LVTTL	SSTL_2	60 to 200
CDCV857A	1:10 PLL differential clock driver for DDR 200/266/333, SSC	SSTL_2/ LVTTL	SSTL_2	60 to 180
CDCV857B	1:10 PLL differential clock driver for DDR 200/266/333, SSC	SSTL_2/ LVTTL	SSTL_2	60 to 200
CDCV857BI	1:10 PLL differential clock driver for DDR 200/266/333, SSC	SSTL_2/ LVTTL	SSTL_2	60 to 200
CDCVF857	1:10 PLL differential clock driver for DDR 200/266/333/400, SSC	SSTL_2/ LVTTL	SSTL_2	60 to 220
DDR Register				
SN74SSTV16857	14-bit registered buffer with SSTL_2 inputs and outputs	SSTL_2	SSTL_2	0 to 200
SN74SSTV16859	13-bit to 26-bit registered buffer with SSTL_2 inputs and outputs	SSTL_2	SSTL_2	0 to 200
SN74SSTV32852	24-bit to 48-bit registered buffer with SSTL_2 inputs and outputs	SSTL_2	SSTL_2	0 to 200
SN74SSTVF16857	14-bit registered buffer with SSTL_2 inputs and outputs	SSTL_2	SSTL_2	0 to 250
SN74SSTVF16859	13-bit to 26-bit registered buffer with SSTL_2 inputs and outputs	SSTL_2	SSTL_2	0 to 500
SN74SSTVF32852	24-bit to 48-bit registered buffer with SSTL_2 inputs and outputs	SSTL_2	SSTL_2	0 to 500
DDR2 PLL				
CDCU877	1:10 PLL differential clock driver for DDR2 applications, SSC	SSTL_18	SSTL_18	10 to 400
CDCU877A	1:10 PLL differential clock driver for DDR2 applications, SSC	SSTL_18	SSTL_18	10 to 400
CDCU877B	1:10 PLL differential clock driver for DDR2 400/533, SSC	SSTL_18	SSTL_18	10 to 340
CDCUA877	1:10 PLL differential clock driver for DDR2 400~800, SSC, 8-mA output	SSTL_18	SSTL_18	125 to 410
CDCU2A877	1:10 PLL differential clock driver for DDR2 400~800, SSC, 16-mA output	SSTL_18	SSTL_18	125 to 410
DDR2 Register				
SN74SSTU32864	25-bit configurable registered buffer with SSTL_18 inputs and outputs	SSTL_18	SSTL_18	0 to 500
SN74SSTU32864C	25-bit configurable registered buffer with SSTL_18 inputs and outputs	SSTL_18	SSTL_18	0 to 500
SN74SSTU32864D	25-bit configurable registered buffer with SSTL_18 inputs and outputs	SSTL_18	SSTL_18	0 to 500
SN74SSTU32864E	25-bit configurable registered buffer with SSTL_18 inputs and outputs	SSTL_18	SSTL_18	0 to 500
SN74SSTU32866	25-bit configurable registered buffer with address-parity test	SSTL_18	SSTL_18	0 to 500
SN74SSTU32866A	25-bit configurable registered buffer with address-parity test	SSTL_18	SSTL_18	0 to 500
SN74SSTUB32864	25-bit configurable registered buffer with SSTL_18 inputs and outputs	SSTL_18	SSTL_18	0 to 410
SN74SSTUB32866	25-bit configurable registered buffer with address-parity test	SSTL_18	SSTL_18	0 to 410
74SSTUB32864A	25-bit configurable registered buffer with SSTL_18 inputs and outputs	SSTL_18	SSTL_18	0 to 410
74SSTUB32866A	25-bit configurable registered buffer with address-parity test	SSTL_18	SSTL_18	0 to 410
74SSTUB32865	26-bit to 56-bit registered buffer with address-parity test	SSTL_18	SSTL_18	0 to 410
74SSTUB32865A	26-bit to 56-bit registered buffer with address-parity test, 12-mA output	SSTL_18	SSTL_18	0 to 410
74SSTUB32868	26-bit to 56-bit registered buffer with address-parity test	SSTL_18	SSTL_18	0 to 410
74SSTUB32868A	26-bit to 56-bit registered buffer with address-parity test, 12-mA output	SSTL_18	SSTL_18	0 to 410
SN74SSTEB32866	25-bit configurable registered buffer with address-parity test	SSTL_18	SSTL_18	0 to 410
DDR3 Register				
SN74SSQE32882	28-bit to 56-bit registered buffer with address-parity test and clock driver	SSTL_15	SSTL_15	300 to 670

New products are listed in bold red. Preview products are listed in bold blue.

Clocks by Application

(Device parameters continued from previous page.)

Device	V_{CC} (V)	Jitter (Peak-to-Peak [P-P] or Cycle-to-Cycle [C-C])	Phase Error	Output Skew (max) (ps)	Char. Temp. (°C)	Package(s)	Price*
SDR							
CDCVF2509A	3.3	C-C: l65l ps (typ) (100 to 166 MHz)	±125 ps (66 to 166 MHz)	100	0 to 85	24/TSSOP	2.40
CDCVF2510A	3.3	C-C: l65l ps (typ) (100 to 166 MHz)	±125 ps (66 to 166 MHz)	100	0 to 85	24/TSSOP	2.40
DDR PLL							
CDCV850	2.5	C-C: ±30 ps (100 to 133 MHz)	–80/150 ps (133 MHz)	75	–40 to 85	48/TSSOP	1.65
CDCV855	2.5	C-C: ±50 ps (100 to 180 MHz)	±100 ps (100 to 180 MHz)	50	–40 to 85	28/TSSOP	1.60
CDCV857	2.5	C-C: ±75 ps (100 to 200 MHz)	–150/50 ps (200 MHz)	75	0 to 85	48/TSSOP	3.90
CDCV857A	2.5	C-C: ±50 ps (100 to 180 MHz)	±100 ps (100 to 180 MHz)	75	0 to 85	48/TSSOP, 56/µBGA[1]	2.65
CDCV857B	2.5	C-C: ±50 ps (100 to 200 MHz)	±50 ps (min/max) (100 to 200 MHz)	70 (typ)	0 to 70	48/TSSOP, 56/µBGA[1]	3.35
CDCV857BI	2.5	C-C: ±50 ps (100 to 200 MHz)	±50 ps (min/max) (100 to 200 MHz)	70 (typ)	–40 to 85	48/TSSOP, 56/µBGA[1]	3.35
CDCVF857	2.5	C-C: ±35 ps (133 to 200 MHz)	±50 ps (min/max) (100 to 200 MHz)	40	–40 to 85	48/TSSOP, 48/QFN, 56/ µBGA[1]	3.35
DDR Register							
SN74SSTV16857	2.5	—	—	—	0 to 70	48/TSSOP	1.95
SN74SSTV16859	2.5	—	—	—	0 to 70	64/TSSOP, 56/QFN	2.55
SN74SSTV32852	2.5	—	—	—	0 to 70	114/LFBGA	5.10
SN74SSTVF16857	2.5	—	—	—	0 to 70	48/TSSOP	1.95
SN74SSTVF16859	2.5	—	—	—	0 to 70	64/TSSOP, 56/QFN	2.55
SN74SSTVF32852	2.5	—	—	—	0 to 70	114/LFBGA	5.10
DDR2 PLL							
CDCU877	1.8	C-C: ±30 ps (190 to 340 MHz)	±50 ps	35	–40 to 85	52/56/µBGA[1], 40/QFN	2.80
CDCU877A	1.8	C-C: ±30 ps (190 to 340 MHz)	±50 ps	35	–40 to 85	52/56/µBGA[1], 40/QFN	2.80
CDCU877B	1.8	C-C: ±30 ps (190 to 340 MHz)	±50 ps	25	–40 to 85	52/µBGA[1]	2.80
CDCUA877	1.8	C-C: ±40 ps (200 to 333 MHz)	±50 ps	35	–40 to 85	52/µBGA[1]	3.10
CDCU2A877	1.8	C-C: ±40 ps (160 to 410 MHz)	±50 ps	35	0 to 70	52/µBGA[1]	3.10
DDR2 Register							
SN74SSTU32864	1.8	—	—	—	0 to 70	96/LFBGA	6.15
SN74SSTU32864C	1.8	—	—	—	0 to 70	96/LFBGA	6.15
SN74SSTU32864D	1.8	—	—	—	0 to 70	96/LFBGA	6.15
SN74SSTU32864E	1.8	—	—	—	0 to 70	96/LFBGA	6.15
SN74SSTU32866	1.8	—	—	—	0 to 70	96/LFBGA	7.10
SN74SSTU32866A	1.8	—	—	—	0 to 70	96/LFBGA	7.10
SN74SSTUB32864	1.8	—	—	—	–40 to 85	96/LFBGA	3.80
SN74SSTUB32866	1.8	—	—	—	–40 to 85	96/LFBGA	3.80
74SSTUB32864A	1.8	—	—	—	0 to 70	96/LFBGA	3.80
74SSTUB32866A	1.8	—	—	—	–40 to 85	96/LFBGA	3.80
74SSTUB32865	1.8	—	—	—	–40 to 85	160/TFBGA	6.15
74SSTUB32865A	1.8	—	—	—	–40 to 85	160/TFBGA	6.15
74SSTUB32868	1.8	—	—	—	–40 to 85	176/VFBGA	6.15
74SSTUB32868A	1.8	—	—	—	–40 to 85	176/VFBGA	6.15
SN74SSTEB32866	1.5	—	—	—	–40 to 85	96/LFBGA	TBD
DDR3 Register							
SN74SSQE32882	1.5	C-C: ±40 ps	±50 ps	–100, +200	0 to 85	176/BGA	5.90

[1] *MicroStar BGA™.* **Suggested resale price in U.S. dollars in quantities of 1,000*

New products are listed in bold red. Preview products are listed in bold blue.

Clocks by Application

Digital Media Systems

(Device parameters continued on next page.)

Device	Description	Input Level	Output Level	Frequency (MHz)
Audio/Video/IP-TV/IP-STB/Streaming Media				
CDCE906	Programmable 3-PLL clock generator with EEPROM	Crystal/single-ended/differential	2.5 to 3.3-V LVTTL	<167
CDC5806	3-PLL-based clock generator for digital TV applications	LVTTL	LVTTL	12 to 74
CDCVF2505	1:5 PLL clock driver for general purpose, SSC	LVTTL	LVTTL	24 to 200
CDCR83A	400-MHz Direct Rambus clock generator, SSC	CMOS	RSL6 (Rambus signaling)	267 to 400
CDCFR83A	533-MHz Direct Rambus clock generator, SSC	CMOS	RSL6 (Rambus signaling)	267 to 533
CDC906	Programmable 3-PLL clock generator	Crystal/single-ended/differential	2.5 to 3.3-V LVTTL	<167
CDCE949	Programmable 4-PLL clock synthesizer with VCXO input	Crystal/VCXO/single-ended	LVTTL	<230
CDCDLP223	Clock synthesizer for DLP®	Crystal	LVTTL/HCLK	20 to 400
CDCD5704	XDR clock generator	HCLK	XDR RSL	300 to 667
CDCE937	Programmable 3-PLL synthesizer with VCXO	Crystal/single-ended/differential	2.5 to 3.3-V LVTTL	<230
CDCE925	Programmable 2-PLL synthesizer with VCXO	Crystal/single-ended/differential	2.5 to 3.3-V LVTTL	<230
CDCE913	Programmable 2-PLL synthesizer with VCXO	Crystal/single-ended/differential	2.5 to 3.3-V LVTTL	<230
CDCS502	1:1 SSC multiplier	Crystal	LVTTL	8 to 108
CDCS503	1:1 SSC multiplier	LVCMOS	LVTTL	DC to 110
DSP and DaVinci™ Clocks				
CDCV304	1:4 fanout for PCI-X and general apps	LVTTL	LVCMOS	0 to 200
CDCVF2505	1:5 PLL clock driver for general purpose, SSC	LVTTL	LVTTL	24 to 200
CDCVF2310	1:10 clock with 2 banks for general-purpose apps, series resistors	LVTTL/LVCMOS	LVTTL/LVCMOS	0 to 170 (VDD = 2.5 V), 0 to 200 (VDD = 3.3 V)
CDCE706	Programmable 3-PLL clock generator with EEPROM	Crystal/single-ended/differential	2.5 to 3.3-V LVTTL	<300
CDCE906	Programmable 3-PLL clock generator with EEPROM	Crystal/single-ended/differential	2.5 to 3.3-V LVTTL	<167
CDCE913	1.8-V programmable 1-PLL VCXO clock synthesizer with 3.3-V outputs	Crystal/VCXO/single-ended	3.3-V LVTTL	<230
CDCEL913	1.8-V programmable 1-PLL VCXO clock synthesizer with 1.8-V outputs	Crystal/VCXO/single-ended	1.8-V LVTTL	<230
CDCE925	1.8-V programmable 2-PLL VCXO clock synthesizer with 3.3-V outputs	Crystal/VCXO/single-ended	3.3-V LVTTL	<230
CDCEL925	1.8-V programmable 2-PLL VCXO clock synthesizer with 1.8-V outputs	Crystal/VCXO/single-ended	1.8-V LVTTL	<230
CDCE937	1.8-V programmable 3-PLL VCXO clock synthesizer with 3.3-V outputs	Crystal/VCXO/single-ended	3.3-V LVTTL	<230
CDCEL937	1.8-V programmable 3-PLL VCXO clock synthesizer with 1.8-V outputs	Crystal/VCXO/single-ended	1.8-V LVTTL	<230
CDCE949	1.8-V programmable 4-PLL VCXO clock synthesizer with 3.3-V outputs	Crystal/VCXO/single-ended	3.3-V LVTTL	<230
CDCEL949	1.8-V programmable 4-PLL VCXO clock synthesizer with 1.8-V outputs	Crystal/VCXO/single-ended	1.8-V LVTTL	<230
Gaming Console				
CDCR83A	400-MHz Direct Rambus clock generator, SSC	CMOS	RSL6 (Rambus signaling)	267 to 400
CDCFR83A	533-MHz Direct Rambus clock generator, SSC	CMOS	RSL6 (Rambus signaling)	267 to 533
CDCD5704	XDR clock generator	HCLK	XDR RSL	300 to 667
Office Automation				
CDCE906	Programmable 3-PLL clock generator with EEPROM	Crystal/single-ended/differential	2.5- to 3.3-V LVTTL	<167
CDCE706	Programmable 3-PLL clock generator with EEPROM	Crystal/single-ended/differential	2.5- to 3.3-V LVTTL	<300
CDCVF2505	1:5 PLL clock driver for general purpose, SSC	LVTTL	LVTTL	24 to 200
CDCE913	1.8-V programmable 1-PLL VCXO clock synthesizer with 3.3-V outputs	Crystal/VCXO/single-ended	3.3-V LVTTL	<230
CDCE925	1.8-V programmable 2-PLL VCXO clock synthesizer with 3.3-V outputs	Crystal/VCXO/single-ended	3.3-V LVTTL	<230
CDCE937	1.8-V programmable 3-PLL VCXO clock synthesizer with 3.3-V outputs	Crystal/VCXO/single-ended	3.3-V LVTTL	<230
CDCE949	1.8-V programmable 4-PLL VCXO clock synthesizer with 3.3-V outputs	Crystal/VCXO/single-ended	3.3-V LVTTL	<230

New products are listed in bold red.

Clocks by Application

(Device parameters continued from previous page.)

Device	V_{CC} (V)	Jitter (Peak-to-Peak [P-P] or Cycle-to-Cycle [C-C])	Phase Error	Output Skew (max) (ps)	Char. Temp. (°C)	Package(s)	Price*
Audio/Video/IP-TV/IP-STB/Streaming Media							
CDCE906	3.3	60 ps (typ)	—	200	0 to 70	20/TSSOP	2.20
CDC5806	3.3	P-P: 150 ps	—	—	–40 to 85	20/TSSOP	2.15
CDCVF2505	3.3	C-C: 70 ps (typ) (66 to 200 MHz)	—	150	–40 to 85	8/TSSOP/SOIC	0.75
CDCR83A	3.3	C-C: 50 ps (400 MHz)	±100 ps	—	–40 to 85	24/SSOP	1.75
CDCFR83A	3.3	C-C: 40 ps (533 MHz)	±100 ps	—	–40 to 85	24/SSOP	2.00
CDC906	3.3	60 ps (typ)	—	200	0 to 70	20/TSSOP	2.20
CDCE949	1.8/2.5 to 3.3	60 ps (typ)	—	150	–40 to 85	24/TSSOP	2.35
CDCDLP223	3.3	Period jitter: ±75 ps	—	—	0 to 70	20/TSSOP	2.90
CDCD5704	2.5	C-C: 40 ps (300 to 635 MHz)	—	—	0 to 70	28/TSSOP	2.95
CDCE937	1.8/2.5 to 3.3	60 ps (typ)	—	150	–40 to 85	20/TSSOP	2.15
CDCE925	1.8/2.5 to 3.3	60 ps (typ)	—	150	–40 to 85	16/TSSOP	1.80
CDCE913	1.8/2.5 to 3.3	60 ps (typ)	—	150	–40 to 85	14/TSSOP	1.60
CDCS502	3.3	60 ps (typ)	—	—	–40 to 85	8/TSSOP	0.95
CDCS503	3.3	60 ps (typ)	—	—	–40 to 85	8/TSSOP	0.95
DSP and DaVinci™ Clocks							
CDCV304	3.3	—	1.8 to 3.0-ns propagation delay	100	–40 to 85	8/TSSOP	1.10
CDCVF2505	3.3	C-C: 70 ps (typ) (66 to 200 MHz)	—	150	–40 to 85	8/TSSOP/SOIC	0.75
CDCVF2310	2.5/3.3	—	1.3 to 2.8-ns propagation delay	100	–40 to 85	24/TSSOP	2.05
CDCE706	3.3	60 ps (typ)	—	200	–40 to 85	20/TSSOP	3.60
CDCE906	3.3	60 ps (typ)	—	200	0 to 70	20/TSSOP	2.20
CDCE913	1.8/2.5 to 3.3	60 ps (typ)	—	150	–40 to 85	14/TSSOP	1.60
CDCEL913	1.8/2.5 to 3.3	60 ps (typ)	—	150	–40 to 85	14/TSSOP	1.60
CDCE925	1.8/2.5 to 3.3	60 ps (typ)	—	150	–40 to 85	16/SSOP	1.80
CDCEL925	1.8/2.5 to 3.3	60 ps (typ)	—	150	–40 to 85	16/SSOP	1.80
CDCE937	1.8/2.5 to 3.3	60 ps (typ)	—	150	–40 to 85	20/TSSOP	2.15
CDCEL937	1.8/2.5 to 3.3	60 ps (typ)	—	150	–40 to 85	20/TSSOP	2.15
CDCE949	1.8/2.5 to 3.3	60 ps (typ)	—	150	–40 to 85	24/TSSOP	2.35
CDCEL949	1.8/2.5 to 3.3	60 ps (typ)	—	150	–40 to 85	24/TSSOP	2.35
Gaming Console							
CDCR83A	3.3	C-C: 50 ps (400 MHz)	±100 ps	—	–40 to 85	24/SSOP	1.75
CDCFR83A	3.3	C-C: 40 ps (533 MHz)	±100 ps	—	–40 to 85	24/SSOP	2.00
CDCD5704	2.5	C-C: 40 ps (300 to 635 MHz)	—	—	0 to 70	28/TSSOP	2.95
Office Automation							
CDCE906	3.3	60 ps (typ)	—	200	0 to 70	20/TSSOP	2.20
CDCE706	3.3	60 ps (typ)	—	200	–40 to 85	20/TSSOP	3.60
CDCVF2505	3.3	C-C: 70 ps (typ) (66 to 200 MHz)	—	150	–40 to 85	8/TSSOP/SOIC	0.75
CDCE913	1.8	60 ps (typ)	—	150	–40 to 85	14/TSSOP	1.60
CDCE925	1.8	60 ps (typ)	—	150	–40 to 85	16/TSSOP	1.80
CDCE937	1.8	60 ps (typ)	—	150	–40 to 85	20/TSSOP	2.15
CDCE949	1.8	60 ps (typ)	—	150	–40 to 85	24/TSSOP	2.35

Suggested resale price in U.S. dollars in quantities of 1,000.

New products are listed in bold red.

Clocks by Application

Data Communications (Ethernet, 1G Ethernet, 10G Ethernet, Fibre Channel, PCI Express, Serial ATA) (Device parameters continued on next page.)

Device	Description	Input Level	Output Level	Frequency (MHz)
Clock Generator/Jitter Cleaner				
CDCE62005	3:5 generator/jitter cleaner with integrated VCO	Crystal/differential/ single-ended	LVPECL/LVDS/LVCMOS	4.25 to 1175
CDCE72010	2:10 synchronizer/jitter cleaner with external VCXO	Differential/single-ended	LVPECL/LVDS/LVCMOS	0 to 1250
CDCM7005	Synchronizer/jitter cleaner with external VCXO	Differential/single-ended	LVPECL/LVCMOS	0 to 1500
CDCE421	Clock genrator with integrated VCO	Crystal/single-ended	LVPECL	11 to 1100
CDCE706	3-PLL programmble clock synthesizer with EEPROM	Crystal/differential/ single-ended	2.5-V/3.3-V LVTTL	0 to 300
CDCM61001/002/004	1:1/1:2/1:4 generator with integrated VCO	Crystal/differential/ single-ended	LVPECL/LVDS/LVCMOS	62.5, 74.5, 75, 100, 106.25, 125, 150, 155.52, 156.25, 212.5, 250, 311.04, 312.5, 622.08, 625; LVCMOS output frequency up to 250 MHz
Buffers				
CDCE18005	1:5 buffer with divider	Differential/Single-ended	LVPECL/LVDS/ LVCMOS	0 to 1500
CDCLVP215	Dual 1:5 LVPECL buffer	LVPECL	LVPECL	0 to 3500
CDCLVP111	1:10 LVPECL buffer with input mux	LVPECL	LVPECL	0 to 3500
CDCLVP110	1:10 LVPECL/HSTL with selectable input clock	LVPECL/HSTL	LVPECL	0 to 3500
CDCLVD110A	1:10 programmable LVDS buffer	LVDS	LVDS	0 to 900
CDCVF111	1:9 LVPECL buffer	LVPECL	LVPECL	0 to 650
CDCP1803	1:3 LVPECL buffer with divider	LVPECL/LVDS	LVPECL	0 to 800
CDCM1804	1:3 LVPECL + 1:1 LVCMOS buffer with divider	LVPECL	LVPECL/LVCMOS	0 to 800
CDCM1802	1:1 LVPECL + 1:1 LVCMOS buffer with divider	LVPECL	LVPECL/LVCMOS	0 to 800
CDCL1810	1:10 CML buffer	LVDS	CML	0 to 650
CDCV304	1:4 LVCMOS buffer	Single-ended	LVCMOS	0 to 200
CDCVF310	1:10 buffer			0 to 200
CDCVF2310	1:10 buffer with series output resistor	LVTTL/LVCMOS	LVTTL/LVCMOS	0 to 200 at 3.3 V; 0 to 170 at 2.5 V
CDC318A	1:18 buffer with I^2C control	LVTTL	LVTTL/LVCMOS	0 to 100
CDC351I	1:10 with 3-state output	LVTTL	LVTTL/LVCMOS	0 to 100
CDCVF25081	1:8 low-power PLL clock with two banks, SSC	LVTTL	LVTTL	8 to 200
CDCVF25084	1:8 low-power 4x multiplier with two banks, SSC	LVTTL	LVTTL	10 to 180
Ethernet/10G Ethernet				
CDCM61001/002/004	1:1/1:2/1:4 generator with integrated VCO	Crystal/differential/single-ended	LVPECL/LVDS/LVCMOS	62.5, 74.5, 75, 100, 106.25, 125, 150, 155.52, 156.25, 212.5, 250, 311.04, 312.5, 622.08, 625; LVCMOS output frequency up to 250 MHz
Fibre Channel				
CDCM61001/002/004	1:1/1:2/1:4 generator with integrated VCO	Crystal/differential/single-ended	LVPECL/LVDS/LVCMOS	62.5, 74.5, 75, 100, 106.25, 125, 150, 155.52, 156.25, 212.5, 250, 311.04, 312.5, 622.08, 625; LVCMOS output frequency up to 250 MHz
PCI Express				
CDCM61001/002/004	1:1/1:2/1:4 generator with integrated VCO	Crystal/differential/single-ended	LVPECL/LVDS/LVCMOS	62.5, 74.5, 75, 100, 106.25, 125, 150, 155.52, 156.25, 212.5, 250, 311.04, 312.5, 622.08, 625; LVCMOS output frequency up to 250 MHz
Base-Station Radio Card				
CDCE72010	2:10 synchronizer/jitter cleaner with external VCXO	Differential/single-ended	LVPECL/LVDS/LVCMOS	0 to 1250
CDCE62005	3:5 generator/jitter cleaner with integrated VCO	Crystal/differential/single-ended	LVPECL/LVDS/LVCMOS	4.25 to 1175
CDCM61001/002/004	1:1/1:2/1:4 generator with integrated VCO	Crystal/differential/single-ended	LVPECL/LVDS/LVCMOS	62.5, 74.5, 75, 100, 106.25, 125, 150, 155.52, 156.25, 212.5, 250, 311.04, 312.5, 622.08, 625; LVCMOS output frequency up to 250 MHz
CDCM7005	Synchronizer/jitter cleaner with external VCXO	Differential/single-ended	LVPECL/LVCMOS	0 to 1500

New products are listed in bold red.

(Device parameters continued from previous page.)

Device	V_{CC} (V)	Jitter	Output Skew (ps)	Char. Temp (°C)	Package(s)	*Price
Clock Generator/Jitter Cleaner						
CDCE62005	3.3	<1 ps rms	TBD	–40 to 85	48/QFN	7.50
CDCE72010	3.3	<1 ps rms	50	–40 to 85	64/QFN	10.95
CDCM7005	3.3	<1 ps rms	50	–40 to 85	64/BGA, 48/QFN	10.75
CDCE421	3.3	<1 ps rms	—	–40 to 85	24/QFN	7.70
CDCE706	3.3	60 ps typ	200	–40 to 85	20/TSSOP	3.60
CDCM61001 **CDCM61002** **CDCM61004**	3.3	<1 ps rms	TBD	–40 to 85	20/QFN 28/QFN 32/QFN	4.20 5.00 6.50
Buffers						
CDCE18005	3.3	—	TBD	–40 to 85	48/QFN	5.96
CDCLVP215	2.5/3.3	—	30	–40 to 85	32/LQFP	6.10
CDCLVP111	2.5/3.3	—	30	–40 to 85	32/LQFP	6.10
CDCLVP110	2.5/3.3	—	30	–40 to 85	32/LQFP	6.10
CDCLVD110A	2.5	—	30	–40 to 85	32/LQFP	5.90
CDCVF111	3.3	—	30	–40 to 85	28/PLCC	7.35
CDCP1803	3.3	—	30	–40 to 85	24/QFN	3.15
CDCM1804	3.3	—	30 ps (LVPECL) 1.6 ns (LVCMOS)	–40 to 85	24/QFN	5.50
CDCM1802	3.3	—	30 ps (LVPECL) 1.6 ns (LVCMOS)	–40 to 85	16/QFN	3.75
CDCL1810	1.8	—	64	–40 to 85	48/QFN	6.00
CDCV304	2.5/3.3	—	100	–40 to 85	8/TSSOP	1.10
CDCVF310	2.5/3.3	—	150 ps at 3.3 V; 230 at 2.5 V	–40 to 85	24/TSSOP	2.05
CDCVF2310	2.5/3.3	—	100 ps at 3.3 V; 170 at 2.5 V	–40 to 85	24/TSSOP	2.05
CDC318A	3.3	—	250	–40 to 85	48/SSOP	1.45
CDC351I	3.3	—	600	–40 to 85	24/SOIC/SSOP	5.65
CDCVF25081	3.3	C-C: ±120 ps (75 to 180 MHz)	150	–40 to 85	16/TSSOP	2.45
CDCVF25084	3.3	C-C: ±100 ps (66 to 200 MHz)	150	–40 to 85	16/TSSOP/SOIC	1.25
Ethernet/10G Ethernet						
CDCM61001 **CDCM61002** **CDCM61004**	3.3	<1 ps rms	TBD	-40 to 85	20/QFN 28/QFN 32/QFN	4.20 5.00 6.50
Fibre Channel						
CDCM61001 **CDCM61002** **CDCM61004**	3.3	<1 ps rms	TBD	–40 to 85	20/QFN 28/QFN 32/QFN	4.20 5.00 6.50
PCI Express						
CDCM61001 **CDCM61002** **CDCM61004**	3.3	<1 ps rms	TBD	–40 to 85	20/QFN 28/QFN 32/QFN	4.20 5.00 6.50
Base-Station Radio Card						
CDCE72010	3.3	<1 ps rms	50	–40 to 85	64/QFN	10.95
CDCE62005	3.3	<1 ps rms	TBD	–40 to 85	48/QFN	7.50
CDCM61001 **CDCM61002** **CDCM61004**	3.3	<1 ps rms	TBD	–40 to 85	20/QFN 28/QFN 32/QFN	4.20 5.00 6.50
CDCM7005	3.3	<1 ps rms	50	–40 to 85	64/BGA, 48/QFN	10.75

*Suggested resale price in U.S. dollars in quantities of 1,000.

New products are listed in bold red.

Clocks by Application

Data Communications (Ethernet, 1G Ethernet, 10G Ethernet, Fibre Channel, PCI Express, Serial ATA)

evice	Description	Input Level	Output Level	Frequency (MHz)	V_{CC} (V)	Jitter	Output Skew (ps)	Char. Temp (°C)	Package(s)	*Price
Base-Station Radio Card										
CDCLVP110	1:10 LVPECL/HSTL with selectable input clock	LVPECL/HSTL	LVPECL	0 to 3500	2.5/3.3	—	30	–40 to 85	32/LQFP	5.55
CDCLVD110A	1:10 programmable LVDS buffer	LVDS	LVDS	0 to 900	2.5	—	30	–40 to 85	32/LQFP	5.90
CDCLVP215	Dual 1:5 LVPECL buffer	LVPECL	LVPECL	0 to 3500	2.5/3.3	—	30	–40 to 85	32/LQFP	6.25
CDCLVP111	1:10 LVPECL buffer with input mux	LVPECL	LVPECL	0 to 3500	2.5/3.3	—	30	–40 to 85	32/LQFP	6.10
CDCE18005	1:5 buffer with divider	Differential/ single-ended	LVPECL/LVDS/ LVCMOS	0 to 1500	3.3	—	TBD	–40 to 85	48/QFN	5.96
Base-Station Baseband Card										
CDCE62005	3:5 generator/jitter cleaner with integrated VCO	Crystal/differen-tial/single-ended	LVPECL/LVDS/ LVCMOS	4.25 to 1175	3.3	<1 ps rms	TBD	–40 to 85	48/QFN	7.50
CDCE706	3-PLL programmble clock synthesizer with EEPROM	Crystal/differen-tial/single-ended	2.5 V/3.3 V LVTTL	0 to 300	3.3	60 ps typ	200	–40 to 85	20/TSSOP	3.60
CDCL1810	1:10 CML buffer	LVDS	CML	0 to 650	1.8	—	64	–40 to 85	48/QFN	6.00
CDCV304	1:4 LVCMOS buffer	Single-ended	LVCMOS	0 to 200	2.5/3.3	—	100	–40 to 85	8/TSSOP	1.10
CDCVF25084	1:8 low-power 4x multiplier with two banks, SSC	LVTTL	LVTTL	10 to 180	3.3	C-C: ±100 ps (66 to 200 MHz)	150	–40 to 85	16/TSSOP/ SOIC	1.25
CDCVF25081	1:8 low-power PLL clock with two banks, SSC	LVTTL	LVTTL	8 to 200	3.3	C-C: ±120 ps (75 to 180 MHz)	150	–40 to 85	16/TSSOP	2.45

*Suggested resale in U.S. dollars in quantities of 1,000)

New products are listed in bold red.

Real-Time Clocks

Device	V_{CC} Level (V)	V_{CC} Tolerance (%)	CPU Supervisor	Onboard NVSRAM	External NVSRAM Control	Package(s)	*Price
Parallel Interface							
bq4802Y	5	10	Yes	No	Yes	28/SOIC/TSSOP	2.50
bq4802LY	3	10	Yes	No	Yes	28/SOIC/TSSOP	2.50
bq4845	5	5	Yes	No	Yes	28/SOIC	2.50
bq4845Y	5	10	Yes	No	Yes	28/SOIC	2.50
bq4830Y	5	10	No	32K x 8	No	28/DIP Module	10.50
bq4822Y	5	10	No	8K x 8	No	28/DIP Module	9.50
bq4832Y	5	10	No	32K x 8	No	32/DIP Module	12.50
bq4842Y	5	10	No	128K x 8	No	32/DIP Module	14.50
bq4852Y	5	10	No	512K x 8	No	36/DIP Module	29.00
bq4847	5	5	Yes	No	Yes	28/DIP Module	4.95
bq4847Y	5	10	Yes	No	Yes	28/DIP Module	4.95
bq4850Y	5	10	No	512K x 8	No	32/DIP Module	25.00
Address/Data Multiplexed							
bq3285	5	10	No	114 bytes	No	24/SOIC	2.10
bq3285E	5	10	No	242 bytes	No	24/SOIC/SSOP	2.10
bq3285LD	3	10	No	242 bytes	No	24/SSOP	2.10
bq3285LF	3	10	No	240 bytes	No	24/SSOP	2.10
bq3287	5	10	No	114 bytes	No	24/DIP Module	3.80
bq3287A	5	10	No	114 bytes	No	24/DIP Module	3.80
bq3287E	5	10	No	242 bytes	No	24/DIP Module	3.80
bq3287EA	5	10	No	242 bytes	No	24/DIP Module	3.80
bq4285	5	10	No	114 bytes	Yes	24/SOIC	2.35
bq4285E	5	10	No	114 bytes	Yes	24/SOIC	2.35
bq4287	5	10	No	114 bytes	Yes	24/DIP Module	4.30

*Suggested resale price in U.S. dollars in quantities of 1,000.

Literature

Literature

Literature is available to download as Acrobat Reader files at www-s.ti.com/sc/techlit/*litnumber* by replacing *litnumber* with the number shown in the Lit. No. column. Other literature is available at www.ti.com/clockappnotes

For More Information

For more information, please visit http://clocks.ti.com or contact your nearest TI Product Information Center listed on the back cover.

Title	Lit. No.
Defining Skew, Propagation-Delay, Phase Offset (Phase Error)	scaa055
Design and Layout Guidelines for the CDCVF2505 Clock Driver	scaa045
Design Considerations for TI's CDCV857/CDCV857A DDR PLL	scaa054
Filtering Techniques: Isolating Analog and Digital Power Supplies in TI's PLL-Based CDC Devices	scaa048
HSTL Clock Buffer Using the CDCV850	scaa058
Interfacing Between LVPECL, LVDS, and CML	scaa056
Jitter Performance of TI's CDC111/CDCVF111	scaa047
Output Jitter of CDC111/CDCVF111 in an ASIC Networking Application	scaa051
Using the CDC857 and CDCV850 to Transform a Single-Ended Clock Signal Into Differential Outputs	scaa043
Using TI's CDCVF111 with SLK2501 Serial Gigabit Transceiver for SONET and Gigabit Ethernet Applications	scaa050
Using TI's CDC111/CDCVF111 with TLK3104SA Serial Transceiver for Gigabit Ethernet and Backplane Applications	scaa049
Using TI's CDCV304 with Backplane Transceiver (TLK1201/1501/2201/2501/2701/2711/3101)	scaa052
AC-Coupling Between Differential LVPECL, LVDS, HSTL and CML	scaa059
Practical Consideration on Choosing a Crystal for CDCE(L)9xx Family	slea071
Clocking Recommendations for DM6446 Digital Video EVM with Single PLL	scaa084
VCXO Application Guideline for CDCE(L)9xx Family	scaa085
CDCE62005 Phase Noise and Jitter Cleaning Performance	scaa095

Title	Lit. No.
CDCE62005 as Clock Solution for High-Speed ADCs	scaa094
DC-Coupling Between Differential LVPECL, LVDS, HSTL, and CML	scaa062
General Guidelines: CDC7005 as a Clock Synthesizer and Jitter Cleaner	scaa063
Phase noise (Jitter) Performance of CDC7005 with Different VCXOs	scaa067
Using the CDC7005 as a 1:5 PECL Buffer w/Programmable Divider Ratio	scaa060
Basics of the CDC7005 Hold Function	scaa078
Phase Noise/Phase Jitter Performance of CDCM7005	scaa077
Recommended Terminations for the Differential Inputs of CDCE906/CDCE706	scaa081
Termination and Signal Integrity Guidelines	scaa080
Implementing a CDC7005 Low-Jitter Clock Solution for High-Speed, High-IF ADC Dev .	slwa034
PCB Layout Guidelines for CDCLVP110	scaa057
Using TI's CDCVF2310 and CDCVF25081 with TLK1501 Serial Transceiver	scaa064
CDCE72010 as a Clocking Solution for High-Speed Analog-to-Digital Converters	scaa092
Phase Noise Performance and Jitter Cleaning Ability of CDCE72010	scaa091
Using the CDCE72010 as a Frequency Synthesizer	scaa090
LAN and WAN Clock Generation and Muxing Using the CDCE62005	scaa098
Real-Time Clock Notes	**Lit. No.**
U-500 Using the bq4845 for a Low-Cost RTC/NVSRAM Subsystem	slua031
U-502 Time-Base Oscillator for RTC IC	slua051
U-503 Using the bq3285/7E in a Green or Portable Environment	slua094
Using RAM Clear Function with bq3285/bq3287A RTCs	slua052

Part Number	TI Replacement	Code
AMI Semiconductor (Now On-Semi)		
FS612509	CDCVF2509A*, CDCVF2509*	Q
FS6377-01G	CDCE937, CDCE706, CDCE906	F
Analog Devices (ADI)		
AD9510	CDCE72010, CDCM7005	F
AD9512	CDCE18005	F
AD9516	CDCE62005	F
AD9516-3	CDCE62005	F
ADF4110	CDC7005	F
Cypress Semiconductor		
2211QC-1	CDCR81*	Q
B9660	CDC319*	Q
B9680	CDC318A*	Q
B9688	CDC318A*	Q
C9850	CDC930*	Q
CY2212	CDCR61A*	S
CY2220	CDC930*	Q
CY22388	CDCE949, CDCE937, CDCE925	F
CY22389	CDCE949, CDCE937, CDCE925	F
CY22391	CDCE949, CDCE937, CDCE925	F
CY2304NZ	CDCV304*	Q
CY2305	CDCVF2505*	Q
CY2308-1	CDCVF25081*	Q
CY2308-3	CDCVF25084	P
CY2310ANZ	CDC319*	Q
CY2310BNZ	CDC319*	Q
CY2318ANZ	CDC318A*	Q
CY2318BNZ	CDC318A*	Q
CY23S05SC-1	CDCVF2505*	Q
CY23S05SC-1H	CDCVF2505*	Q
CY23S08-1	CDCVF25081*	Q
CY2509	CDCVF2509A*, CDCVF2509*	Q
CY2509ZC-1	CDCVF2509A*	
CY2510	CDCVF2510A*, CDCVF2510*, CDCF2510*	Q
CY26501	CDCFR83*	Q
CY26502	CDCFR83*	Q
CY2SSTV850	CDCV850*	Q
CYSSTV855ZC	CDCV855*	
CYSSTV855ZI	CDCV855I*	
CYSSTV855ZXC	CDCV855*	
CYSSTV855ZXI	CDCV855I*	
CY2SSTV857	CDCV857*, CDCV857A*, CDCV857B*	Q
CY2SSTV857-32	CDCVF857*	Q
CY2SSTV857LFC-32	CDCVF857RHA*	
CY2SSTV857LFI-32	CDCVF857RHA*	
CY2SSTV857ZC-27	CDCVF857DGGR*	
CY2SSTV857ZC-32	CDCVF857DGGR*	
CY2SSTV857ZI-27	CDCVF857DGGR*	
CY2SSTV857ZI-32	CDCVF857DGGR*	
CY2SSTV857ZXC-27	CDCVF857DGGR*	
CY2SSTV857ZXI-27	CDCVF857DGGR*	
CY2SSTV16857ZC	SN74SSTVF16857*	
CY2SSTV16857ZI	SN74SSTVF16857	
CY2SSTV16859LFC	SN74SSTVF16859G4R*	
CY2SSTV16859LFI	SN74SSTVF16859G4R	
CY2SSTV16859ZC	SN74SSTVF16859GR*	
CY2SSTV16859ZI	SN74SSTVF16859GR	
CY2SSTU877BGXC	CDCUA877ZQLR*	
CY2SSTU32866BFXC	SN74SSTUB32866ZKER*	
SC660E	CDC319*	Q
SC680E	CDC318A*	Q
W132-10B	CDCVF2510A*, CDCVF2510*, CDCF2510*	Q
W134M, W134S	CDCR83*	Q

Part Number	TI Replacement	Code
Cypress Semiconductor (cont.)		
W152-1	CDCVF25081*	Q
W152-1/-11	CDCVF25081*	Q
W152-11	CDCVF25081*	Q
W158	CDC924*	Q
W162	CDCVF25081*	Q
W163-05	CDCVF2505*	Q
W163-15	CDCVF2505*	Q
W232-10	CDCVF2510A*, CDCVF2510*, CDCF2510*	Q
W40S01-04	CDC318A*	Q
W40S11-02H	CDC319*	Q
W40S11-02X	CDC319*	Q
Z9305	CDCVF2505*	Q
Z9308-1	CDCVF25081*	Q
Fairchild Semiconductor		
FMS72509	CDCVF2509A*, CDCVF2509*	Q
FMS72510	CDCVF2510A*, CDCVF2510*, CDCF2510*	Q
Hitachi		
HD74CDC2509B	CDCVF2509A*, CDCVF2509*, CDC2509C*	Q
HD74CDC2510B	CDC2510C*, CDCF2510*, CDCVF2510*	Q
HD74CDC857B	CDCV857B*	Q
HD74CDCF2509B	CDCVF2509A*, CDCVF2509*, CDC2509C*	Q
HD74CDCF2510B	CDCVF2510A*, CDCVF2510*, CDCF2510*	Q
HD74CDCV857	CDCV857A*	Q
Inphi		
INCU877	CDCUA877ZQLR*	
INCU878	CDCUA877ZQLR*	
INCUA877	CDCUA877ZQLR*	
INCUA878	CDCUA877ZQLR*	
INSSTE32882	SN74SSQE32882ZALR*	
INSSTU32864	SN74SSTUB32864ZKER*	
INSSTU32866	SN74SSTUB32866ZKER*	
INSSTU32868	74SSTUB32868ZRHR*	
INSSTUA32866	SN74SSTUB32866ZKER*	
INSSTUA32868	74SSTUB32868ZRHR*	
Integrated Device Technology (IDT)		
2305-1	CDCVF2505*	Q
2305-1H	CDCVF2505*	Q
93V850D	CDCV850*	
93V855A	CDCV855*	
CSPT857	CDCV857B*, CDCV857*	Q
CSPT857C	CDCVF857*	Q
CSPU877	CDCU877*	Q
ICS2509C	CDCVF2509A*, CDCVF2509*	Q
ICS2510C	CDCVF2510A*, CDCVF2510*, CDCF2510*	Q
ICS345, ICS343, ICS342, ICS341	CDCE949, CDCE937, CDCE925, CDCE913	F
ICS348	CDCE949, CDCE937, CDCE925, CDCE913	F
ICS477	CDCE949, CDCE937, CDCE925, CDCE913	F
ICS553	CDCV304	P
ICS7151	CDCS502	P
ICS843001	CDCM61001, CDCE421	P
ICS843004	CDCM61004, CDCE62005	P
ICS843034	CDCE62005	F
ICS843252	CDCM61002	F
ICS85310I-01	CDCLVP110, CDCLVP111, CDCLVP215	P
ICS85310I-11	CDCLVP110, CDCLVP111, CDCLVP215	P

Part Number	TI Replacement	Code
Integrated Device Technology (IDT)		
ICS9112-16	CDCVF2505*	Q
ICS9112-17	CDCVF25081*	Q
ICS91305	CDCVF2505*	Q
ICS9179-03	CDC319*	Q
ICS9179B-01	CDC318A*	Q
ICS91857	CDCVF857*	
ICS9211-01	CDCR81*	Q
ICS9212-01	CDCR83	P
ICS9212-02	CDCR83	P
ICS9212-03	CDCR83	P
ICS9212-13	CDCFR83*	Q
ICS9222-01	CDCFR83	P
ICS9248-150	CDC950*	Q
ICS93701	CDCV850*	Q
ICS93716	CDCV855	P
ICS93V847	CDCV855	P
ICS93V857	CDCV857*	Q
ICS95U877	CDCU877*	Q
ICS95V857	CDCVF857*, CDCV857A*, CDCV857B*	Q
ICS95V2F857A	CDCVF857	
ICS95V850	CDCV850*	
ICS97U2A877A	CDCU2A877*	
ICS97U877A	CDCUA877*	
ICS97ULP877A	CDCUA877*	
ICS97ULP877B	CDCUA877*	
ICS97ULPA877A	CDCUA877*	
ICS98UAE877A	CDCUA877*	
ICS98ULPA877A	CDCUA877*	
ICSSSTU32864A	SN74SSTUB32864ZKER*	
ICSSSTUA32864B	SN74SSTUB32864ZKER*	
ICSSSTUA32866B	SN74SSTUB32866ZKER*	
ICSSSTUA32S865B	74SSTUB32865ZJBR*	
ICSSSTUAF32865A	74SSTUB32865ZJBR*	
ICSSSTUAF32866B	SN74SSTUB32866ZKER*	
ICSSSTUAF32866C	SN74SSTUB32866ZKER*	
ICSSSTUAF32868A	74SSTUB32868ZRHR*	
ICSSSTUB32864A	SN74SSTUB32864ZKER*	
ICSSSTUB32866B	SN74SSTUB32866ZKER*	
ICSSSTUB32S865A	74SSTUB32865ZJBR*	
ICSSSTUB32S868B	74SSTUB32868ZRHR*	
ICSSSTUB32S868C	74SSTUB32868ZRHR*	
ICSSSTUB32S868D	74SSTUB32868ZRHR*	
ICSSSTUF32864A	SN74SSTUB32864ZKER*	
ICSSSTUF32864B	SN74SSTUB32864ZKER*	
ICSSSTUF32864C	SN74SSTUB32864ZKER*	
ICSSSTUF32864E	SN74SSTUB32864ZKER*	
ICSSSTUF32866A	SN74SSTUB32866ZKER*	
ICSSSTV16857C	SN74SSTVF16857*	
ICSSSTV16859C	SN74SSTVF16859*	
ICSSSTVA16857A	SN74SSTVF16857*	
ICSSSTVA16859A	SN74SSTVF16859*	
ICSSSTVA16859B	SN74SSTVF16859*	
ICSSSTVA16859C	SN74SSTVF16859*	
ICSSSTVA32852	SN74SSTVF32852*	
ICSSSTVF16857A	SN74SSTVF16857*	
ICSSSTVF16859B	SN74SSTVF16859*	
ICTCSPU877D	CDCUA877*	
IDT74SSTU32864	SN74SSTUB32864ZKER*	
IDT74SSTU32864A	SN74SSTUB32864ZKER*	
IDT74SSTU32864C	SN74SSTUB32864ZKER*	
IDT74SSTU32864D	SN74SSTUB32864ZKER*	
IDT74SSTU32864G	SN74SSTUB32864ZKER*	
IDT74SSTU32865	74SSTUB32865ZJBR*	
IDT74SSTU32866B	SN74SSTUB32866ZKER*	
IDT74SSTU32D868	74SSTUB32868ZRHR*	

New products are listed in bold red.

**Replacement Code Definitions:*
S: The device is a DIRECT REPLACEMENT in functionality, parametrics, and pinout to the competitor's device.
Q: The device has the SAME FUNCTIONALITY AND PINOUT as the competitor's device but is NOT an exact equivalent.
P: The device has the SAME FUNCTIONALITY to the competitor's device, but is not pinout compatible and/or parametrically equivalent.
F: The device has SIMILAR FUNCTIONALITY but is not functionally equivalent to the competitor's device.

Part Number	TI Replacement	Code
Integrated Device Technology (IDT) (cont.)		
IDT74SSTUA32864	SN74SSTUB32864ZKER*	
IDT74SSTUA32866	SN74SSTUB32866ZKER*	
IDT74SSTUAE32866A	SN74SSTUB32866ZKER*	
IDT74SSTUBF32865A	74SSTUB32865ZJBR*	
IDT74SSTUBF32866B	SN74SSTUB32866ZKER*	
IDT74SSTUBF32868A	74SSTUB32868ZRHR*	
IDT74SSTUBH32865A	74SSTUB32865AZJBR*	
IDT74SSTUBH32868A	74SSTUB32868AZRHR*	
IDT74SSTV16857	SN74SSTVF16857*	
IDT74SSTV16859	SN74SSTVF16859*	
IDT74SSTVF16857	SN74SSTVF16857*	
IDT74SSTVF16859	SN74SSTVF16859*	
IDT74SSTVN16859	SN74SSTVF16859*	
IDT74SSTVN16859C	SN74SSTVF16859*	
IDT2308-1	CDCVF25081*	Q
IDT2308-3	CDCVF25084	P
IDTCSP2510C	CDCVF2510A*, CDCVF2510*	Q
IDTCSP2510D	CDCVF2510A*, CDCVF2510*, CDCF2510*	Q
IDTCSPF2510C	CDCVF2510A*, CDCVF2510*, CDCF2510*	Q
IDTCSPT855	CDCV855*	Q
IDTCSPT857	CDCV857*	Q
IDTCSPU877	CDCUA877*	
IDTCSPU877A	CDCUA877*	
IDTCSPUA877	CDCUA877*	
IDTCSPUA877A	CDCUA877*	
MC100ES6111	CDCLVP111*	S
MC100LVEP111	CDCLVP111*	S
MK2069	CDC7005	F
QS5810	CDC319*	Q
QS5818	CDC318A*	Q
SSTE32882HLB	SN74SSQE32882ZALR*	
VF2510B	CDCVF2510A*	
Maxim		
DS1080	CDCS502	P
MAX3610	CDCE62005, CDCE421	F
MAX3622	CDCM61002	P
MAX3624	CDCM61004	P
MAX3629	CDCM61004	P
MAX3670	CDC7005	F
MAX3671	CDCM61004	P
MAX9311	CDCLVP111*	Q
MAX9311	CDCLVP110*	Q
MAX9313	CDCLVP110*	Q
Micrel		
SY100E111A	SN65EL11	
SY100EL16	SN65EL16	
SY100ELT20	SN65ELT20	
SY100E111A	CDC111*	Q
SY100E111A	CDCVF111*	Q
SY100E111L	CDC111*	Q
SY100E111L	CDCVF111*	Q
SY10E111A	CDC111*	Q
SY10E111A	CDCVF111*	Q
SY10E111L	CDCVF111*	Q
SY10E111L	CDC111*	Q
National Semiconductor (NSC)		
LMK02000	CDCE72010	F
LMK03001C	CDCE62005	F
NXP Semiconductor		
PCK1111	CDCLVD110*	Q
PCK2001	CDCR81*	F
PCK2001	CDC318A*	F
PCK2001M	CDC319*	F

Part Number	TI Replacement	Code
NXP Semiconductor (cont.)		
PCK2002	CDC318A*	F
PCK2002M	CDC319*	F
PCK2002P	CDCV304*	F
PCK2002PL	CDCV304*	Q
PCK2020	CDC930*	Q
PCK2022R	CDC950*	Q
PCK2057	CDCV850*	Q
PCK2509S	CDCVF2509A*, CDCVF2509*	Q
PCK2509SA	CDCVF2509A*, CDCVF2509*	S
PCK2509SL	CDCVF2509A*, CDCVF2509*	Q
PCK2510S	CDCVF2510A*, CDCVF2510*	F
PCK2510S	CDCVF2510A*, CDCVF2510*, CDCF2510*	F
PCK2510SA	CDCVF2510A*, CDCVF2510*, CDCF2510*	F
PCK2510SA	CDCVF2510A*, CDCVF2510*	Q
PCK2510SL	CDCVF2510A*, CDCVF2510*, CDCF2510*	Q
PCK2510SL	CDCVF2510A*, CDCVF2510*	Q
PCK857DGG	CDCVF857DGG*	
PCKU877	CDCUA877ZQLR*	
PCKU878	CDCUA877ZQLR*	
PCKV857	CDCV857A*	P
PCKV857A	CDCVF857*	Q
PCKV857DGG	CDCVF857DGG*	
PCKV857DGV	CDCVF857DGG*	
PCKV857EV	CDCVF857ZQLR*	
PCKV857ADGG	CDCVF857DGG*	
PCKV857ADGV	CDCVF857DGG*	
PCKVF857	CDCVF857DGG*	
PTN1111	CDCLVP111*, CDCLVP110*	Q
SSTL16857DGG	SN74SSTVF16857GR*	
SSTL16877DGG	SN74SSTVF16857GR*	
SSTU32864EC	SN74SSTUB32864ZKER*	
SSTU32865ET	74SSTUB32865ZJBR*	
SSTU32866EC	SN74SSTUB32866ZKER*	
SSTUA32864	SN74SSTUB32864ZKER*	
SSTUA32S865	74SSTUB32865ZJBR*	
SSTUA32866	SN74SSTUB32866ZKER*	
SSTUA32S868	74SSTUB32868ZRHR*	
SSTUH32864EC	SN74SSTUB32864ZKER	
SSTUH32865ET	74SSTUB32865AZJBR*	
SSTUH32866EC	SN74SSTUB32866ZWLR	
SSTV16857DGG	SN74SSTVF16857GR*	
SSTV16857ADGG	SN74SSTVF16857GR*	
SSTV16859BS	SN74SSTVF16859G4R*	
SSTVF16857DGG	SN74SSTVF16857GR*	
SSTVF16859BS	SN74SSTVF16859G4R*	
SSTVF16859DGG	SN74SSTVF16859GR*	
SSTVN16859BS	SN74SSTVF16859G4R*	
On Semiconductor		
MC100EL11	SN65EL11	
MC100EL16	SN65EL16	
MC100ELT20	SN65ELT20	
MC100ELT21	SN65ELT21	
MC100EP210	CDCLVP215*	S
MC100ES6111	CDCLVP111*	Q
MC100LVE111	CDC111*	Q
MC100LVE111	CDCVF111*	Q
MC100LVEP111	CDCLVP111*, CDCLVP110*	Q
MC100LVEP210	CDCLVP215*	Q
Pericom Semiconductor		
P16C2108	CDC950*	Q
PI6C2509-133	CDCVF2509A*	
PI6C22510	CDCVF2510A*	

Part Number	TI Replacement	Code
Pericom Semiconductor (cont.)		
PI6C2510-133E	CDCVF2510A*	
PI6C2510A	CDCVF2510A*	
PI6CU877	CDCUA877ZQLR*	
PI6CUA877	CDCUA877ZQLR*	
PI6CV855	CDCV855*	
PI6CV855-02	CDCV855	
PI6CV857	CDCVF857DGGR*	
P16CV857B	CDCV857B*	Q
P16CVF857	CDCVF857*	Q
PI62305-1H, PI62305-1HI	CDCVF2505*	Q
PI6C180, PI6C180A, PI6C180A	CDC318A*	Q
PI6C200	CDCR81*	Q
PI6C2308A-1	CDCVF25081*	Q
PI6C2408-3	CDCVF25084	P
PI6C2509-133	CDCVF2509A*, CDCVF2509*	Q
PI6C2510-133E	CDCVF2510A*, CDCVF2510*, CDCF2510*	Q
PI6C2510-133E	CDCVF2510A*, CDCVF2510*	Q
PI6C2516	CDC516*	*Q*
PI6C2516	CDC2516*	*Q*
PI6CV2304L	CDCV304*	*Q*
PI6CV304L	CDCV304*	*Q*
PI6CV850A	CDCV850*	*Q*
PI6CV855	CDCV855	*P*
PI6CV857	CDCV857A*	*Q*
PI6CV857	CDCV857*	*Q*
PI6CVF857	CDCVF857*	*S*
PI74SSTU32864A	SN74SSTUB32864ZKER*	
PI74SSTUA32864	SN74SSTUB32864ZKER*	
PI74SSTU32866	SN74SSTUB32866ZKER*	
PI74SSTV16857	SN74SSTVF16857GR*	
PI74SSTVF16857	SN74SSTVF16857GR*	
PI74SSTVF16857A	SN74SSTVF16857GR*	
PI74SSTV16859	SN74SSTVF16859GR*	
PI74SSTV16859	SN74SSTVF16859G4R*	
PI74SSTVF16859	SN74SSTVF16859GR*	
PI74SSTVF16859A	SN74SSTVF16859G4R*	
PI74SSTV3285	SN74SSTVF32852ZKFR*	
PI74SSTVF3285	SN74SSTVF32852ZKFR*	
PI74SSTVF3285	SN74SSTVF32852ZKFR*	
PIC182, PIC182A, PIC182B	CDC319*	Q
Semtech Corporation		
SK100EP111	CDCLVP111*, CDCLVP110*	Q
SK2111	CDCLVD110	P
Silego		
SLGVF857C-14F	CDCVF857DGGR*	
SLGVF857C-14V	CDCVF857RHAR*	
SLGSSTVF16857F	SN74SSTVF16857GR*	
SLGSSTVF16859V	SN74SSTVF16859G4R*	
SLGSSTVF16859F	SN74SSTVF16859GR*	
SLGSSTVF16859CF	SN74SSTVF16859GR*	
SLGU877B	CDCUA877ZQLR*	
SLGUA877B	CDCUA877ZQLR*	
SLGSSTUB32864B	SN74SSTUB32864ZKER*	
SLGSSTUB32865B	74SSTUB32865ZJBR*	
SLGSSTUA32866B	SN74SSTUB32866ZKER*	
SLGSSTUB32866B	SN74SSTUB32866ZKER*	
SLGSSTUB32868B	74SSTUB32868ZRHR*	
SLGSSTUE32882B	SN74SSQE32882ZALR*	
ST Microelectronics (STM)		
STLVD111	*CDCLVD110A**	*Q*

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